SCANNED, #24

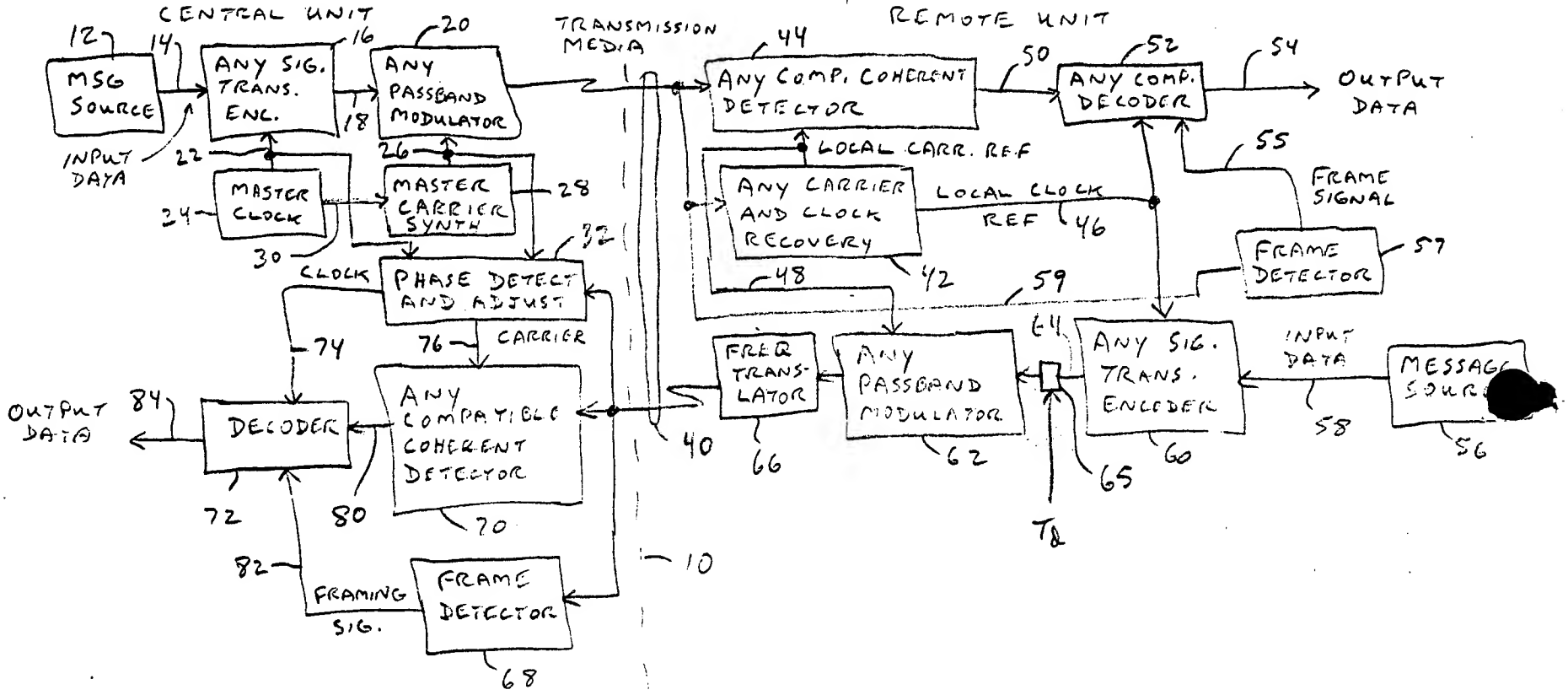


FIG. 1

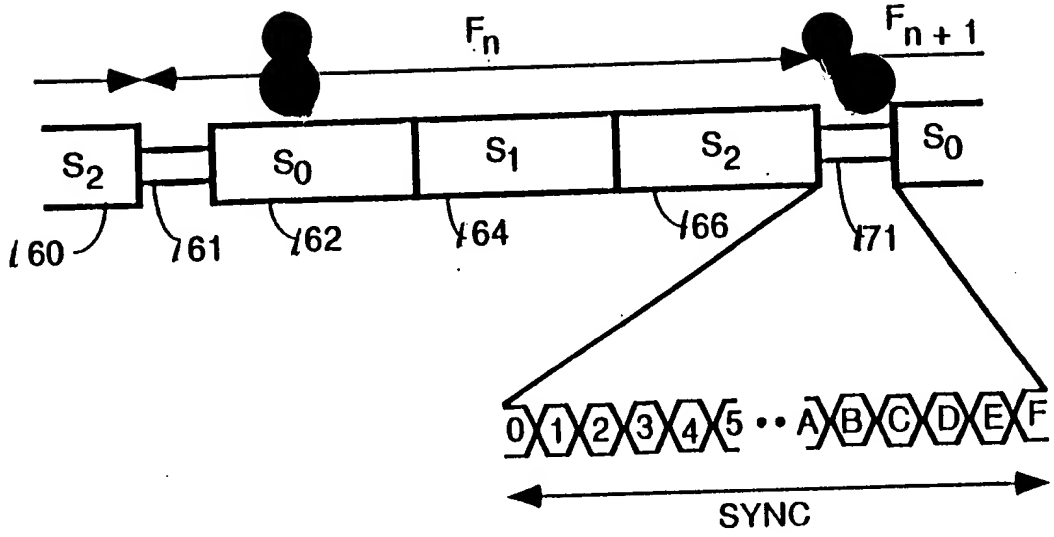

F_n
F_{n+1}
S_2
S_0
S_1
S_2
S_0
160
161
162
164
166
171
0 1 2 3 4 5 • • A B C D E F
SYNC

FIG. 4A

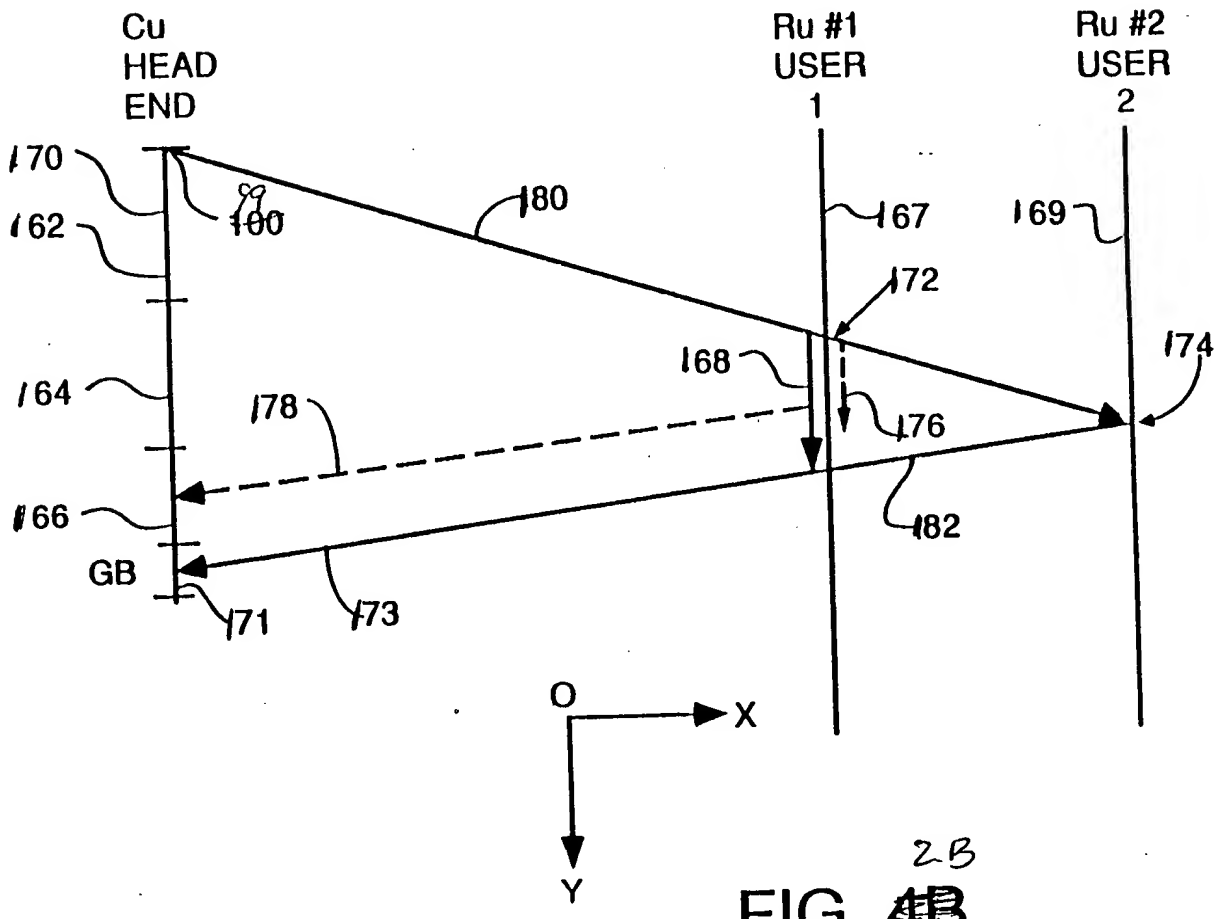

Cu
HEAD
END
Ru #1
USER
1
Ru #2
USER
2
170
162
164
166
GB
171
173
178
180
167
169
172
168
174
176
182
O
X
Y

FIG. 4B

09759774 021102

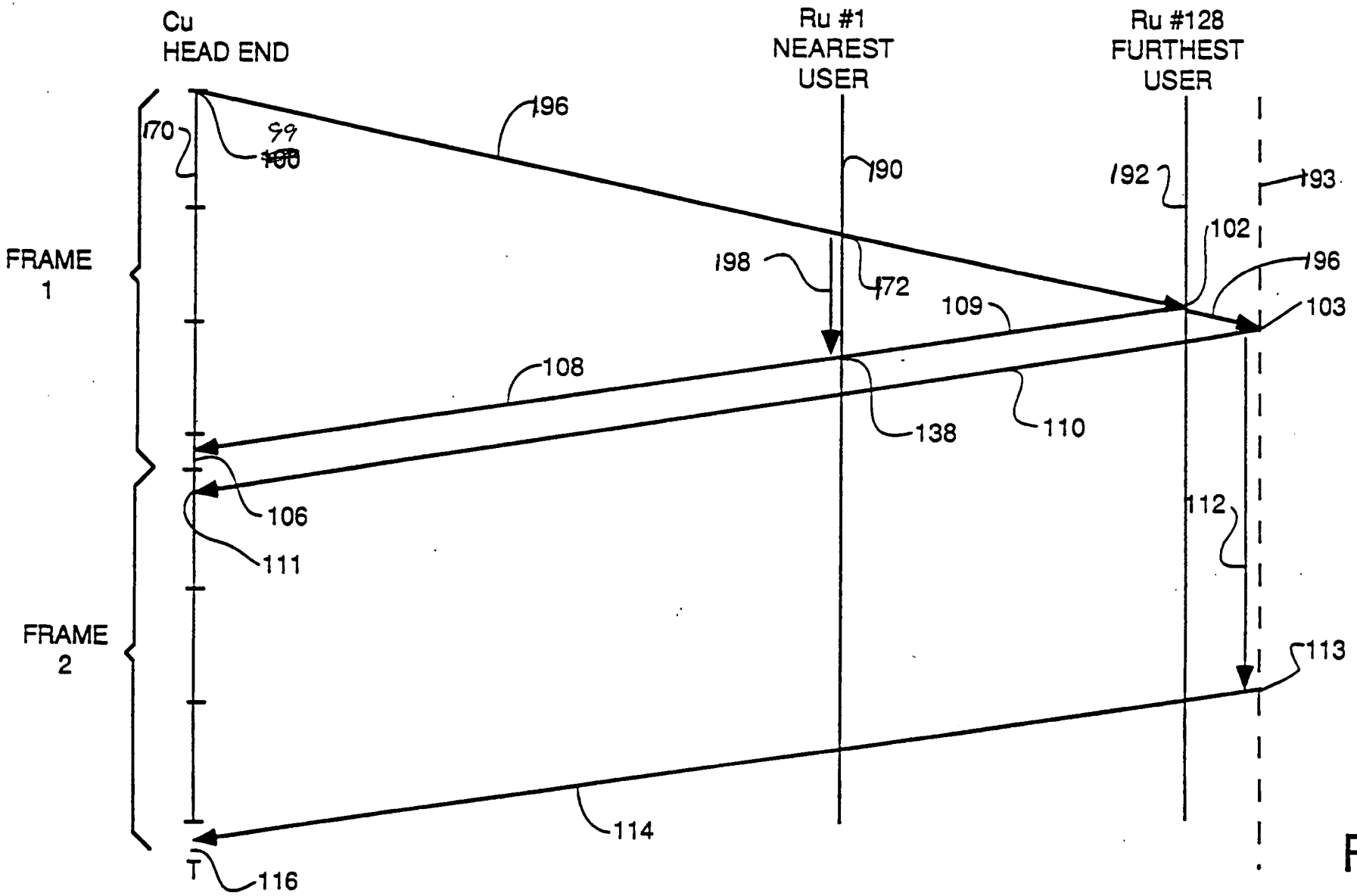


FIG. 3

10211101.442525

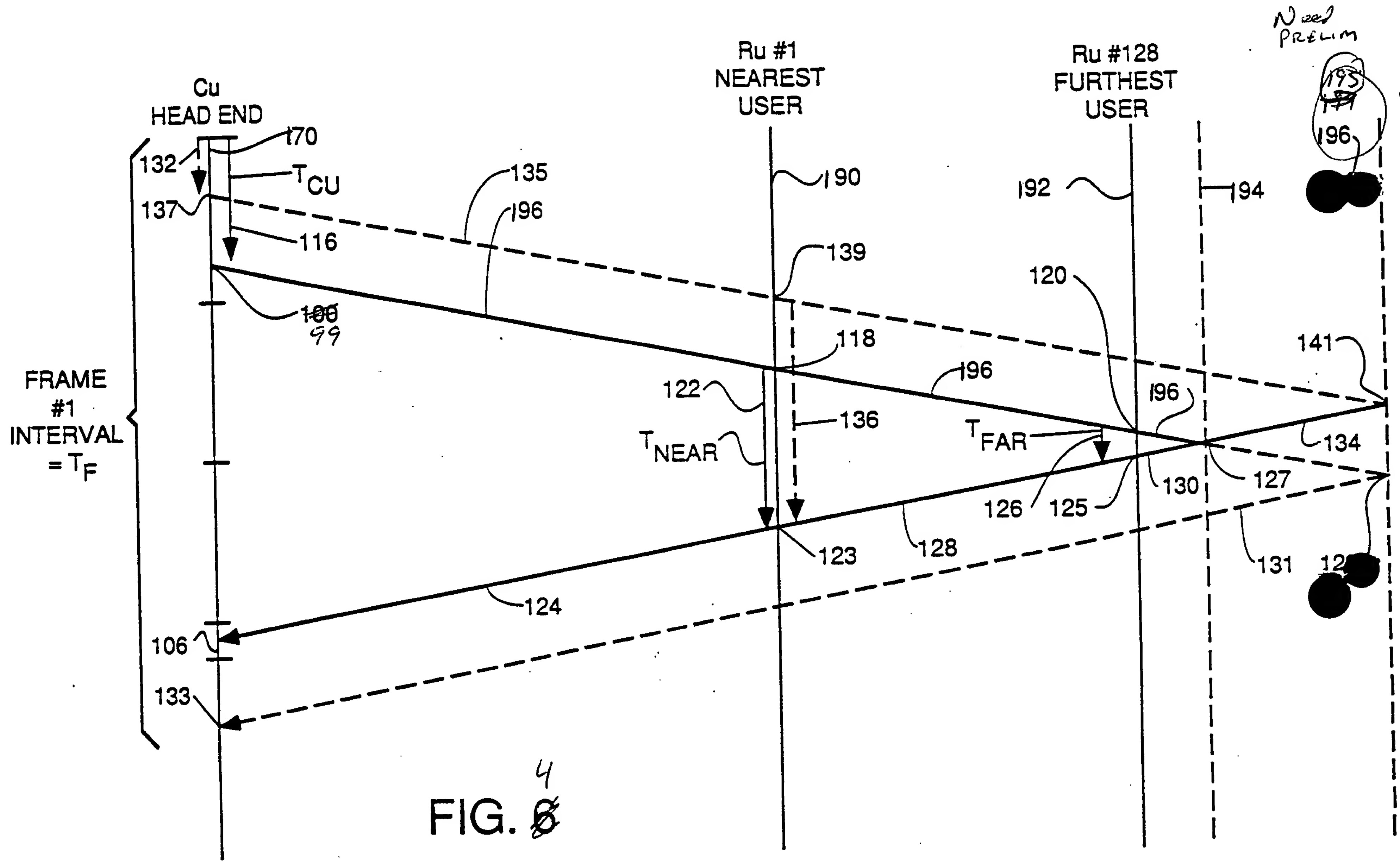
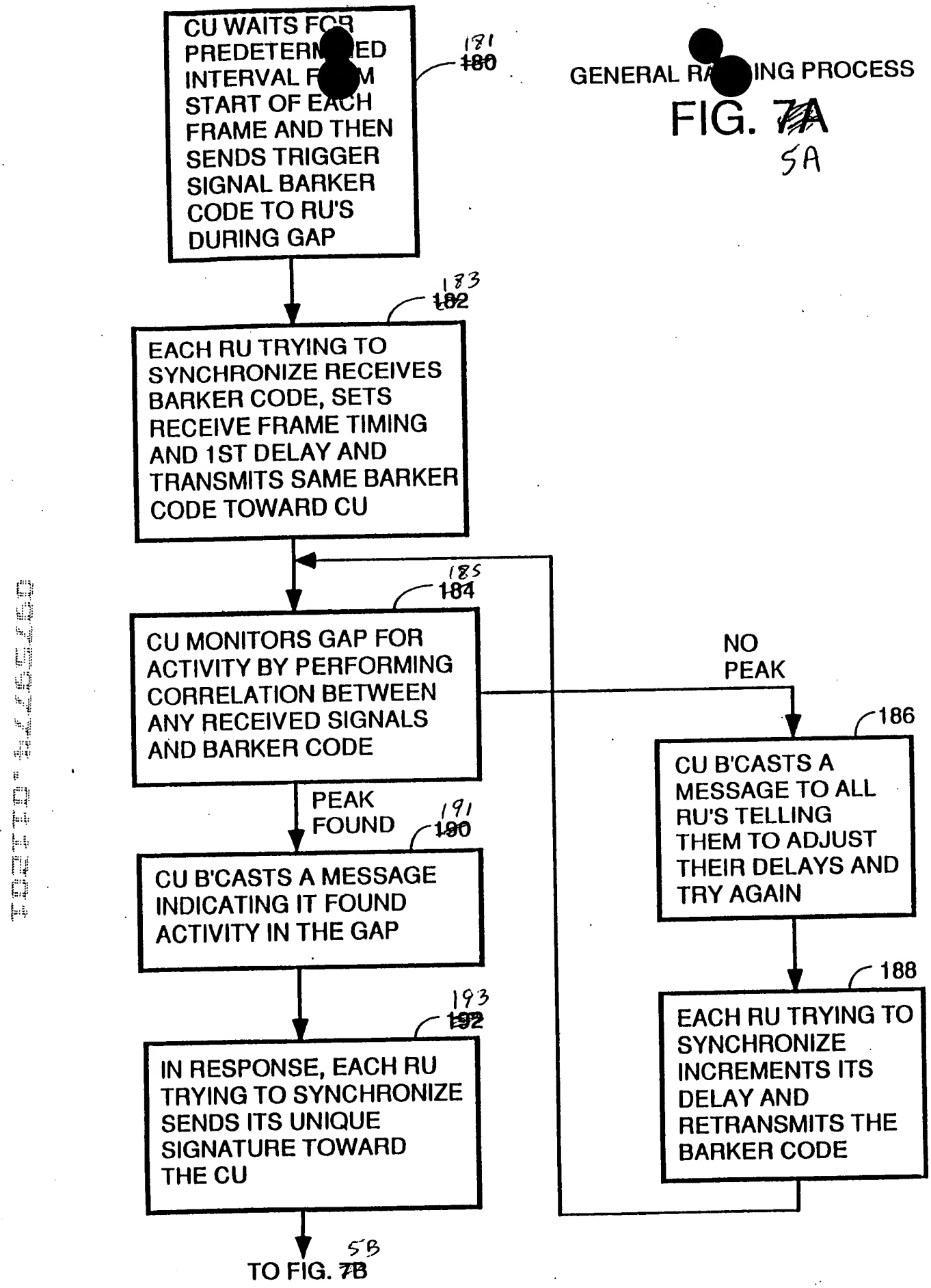


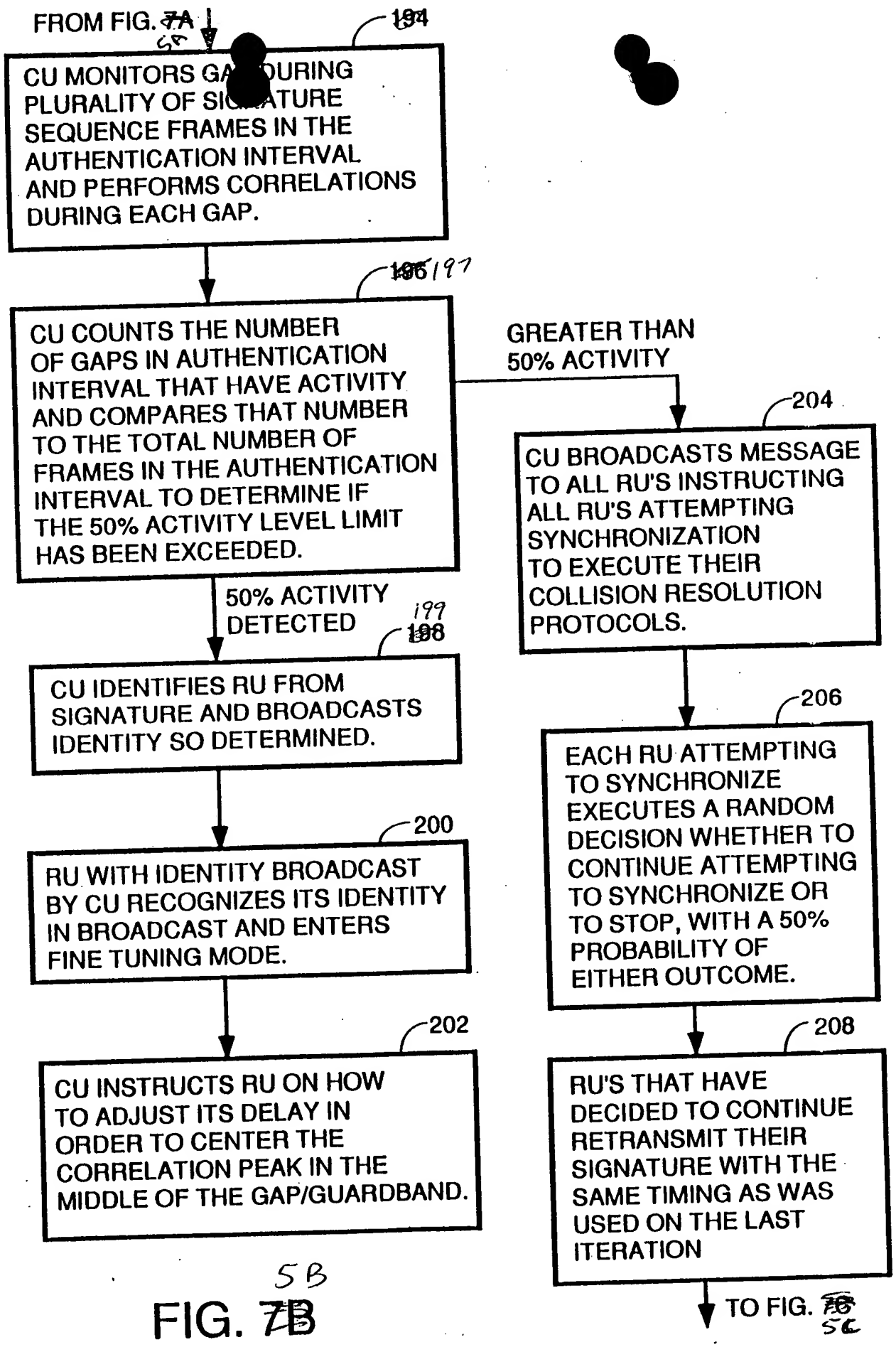
FIG. 4



GENERAL RANGING PROCESS

FIG. 7A

5A


FROM FIG. 7A
5A
194
CU MONITORS GAPS DURING PLURALITY OF SIGNATURE SEQUENCE FRAMES IN THE AUTHENTICATION INTERVAL AND PERFORMS CORRELATIONS DURING EACH GAP.
196/197
CU COUNTS THE NUMBER OF GAPS IN AUTHENTICATION INTERVAL THAT HAVE ACTIVITY AND COMPARES THAT NUMBER TO THE TOTAL NUMBER OF FRAMES IN THE AUTHENTICATION INTERVAL TO DETERMINE IF THE 50% ACTIVITY LEVEL LIMIT HAS BEEN EXCEEDED.
GREATER THAN 50% ACTIVITY
204
CU BROADCASTS MESSAGE TO ALL RU'S INSTRUCTING ALL RU'S ATTEMPTING SYNCHRONIZATION TO EXECUTE THEIR COLLISION RESOLUTION PROTOCOLS.
50% ACTIVITY DETECTED
199
198
CU IDENTIFIES RU FROM SIGNATURE AND BROADCASTS IDENTITY SO DETERMINED.
206
EACH RU ATTEMPTING TO SYNCHRONIZE EXECUTES A RANDOM DECISION WHETHER TO CONTINUE ATTEMPTING TO SYNCHRONIZE OR TO STOP, WITH A 50% PROBABILITY OF EITHER OUTCOME.
200
RU WITH IDENTITY BROADCAST BY CU RECOGNIZES ITS IDENTITY IN BROADCAST AND ENTERS FINE TUNING MODE.
202
CU INSTRUCTS RU ON HOW TO ADJUST ITS DELAY IN ORDER TO CENTER THE CORRELATION PEAK IN THE MIDDLE OF THE GAP/GUARDBAND.
208
RU'S THAT HAVE DECIDED TO CONTINUE RETRANSMIT THEIR SIGNATURE WITH THE SAME TIMING AS WAS USED ON THE LAST ITERATION
TO FIG. 7B
5C

5B

FIG. 7B

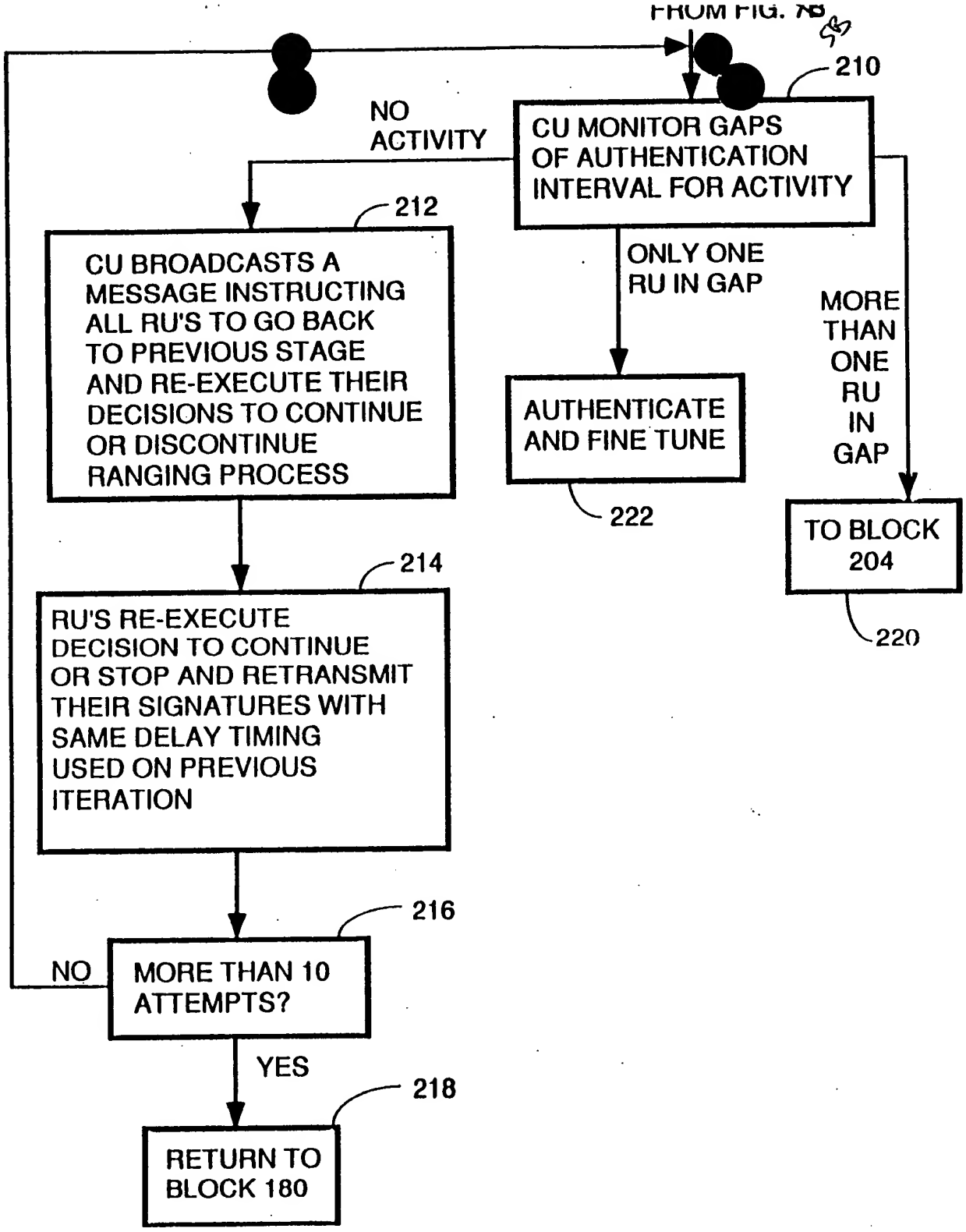
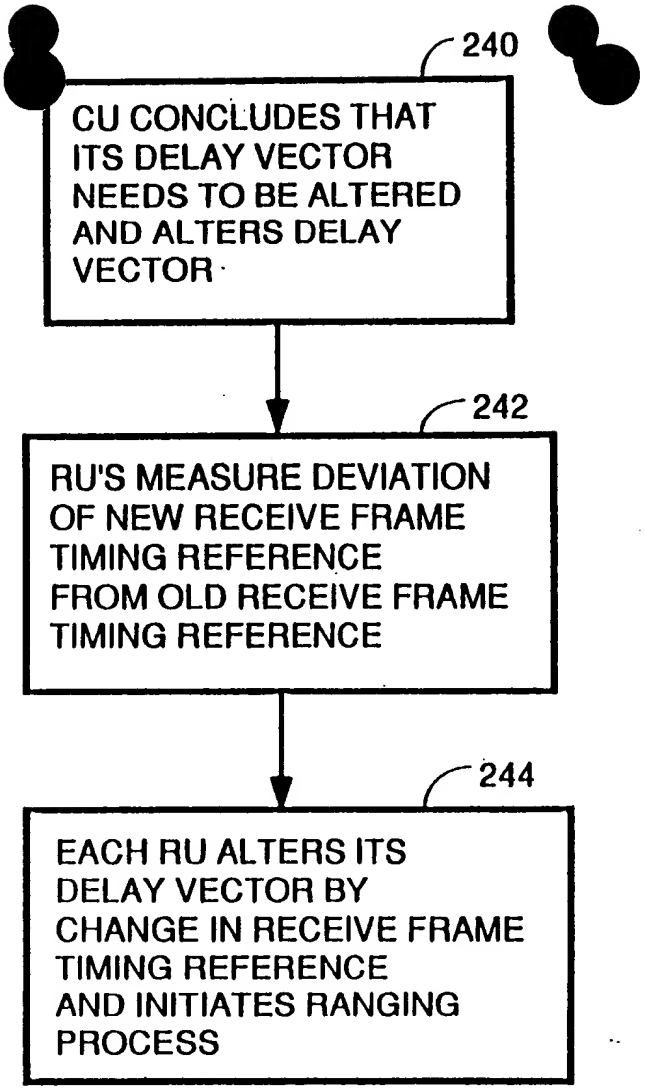

FROM FIG. 5B
210
CU MONITOR GAPS OF AUTHENTICATION INTERVAL FOR ACTIVITY
NO ACTIVITY
212
CU BROADCASTS A MESSAGE INSTRUCTING ALL RU'S TO GO BACK TO PREVIOUS STAGE AND RE-EXECUTE THEIR DECISIONS TO CONTINUE OR DISCONTINUE RANGING PROCESS
ONLY ONE RU IN GAP
AUTHENTICATE AND FINE TUNE
222
MORE THAN ONE RU IN GAP
TO BLOCK 204
220
214
RU'S RE-EXECUTE DECISION TO CONTINUE OR STOP AND RETRANSMIT THEIR SIGNATURES WITH SAME DELAY TIMING USED ON PREVIOUS ITERATION
216
NO
MORE THAN 10 ATTEMPTS?
YES
218
RETURN TO BLOCK 180

FIG. 5C ~~7C~~



6

FIG. 8

DEAD RECKONING RE-SYNC

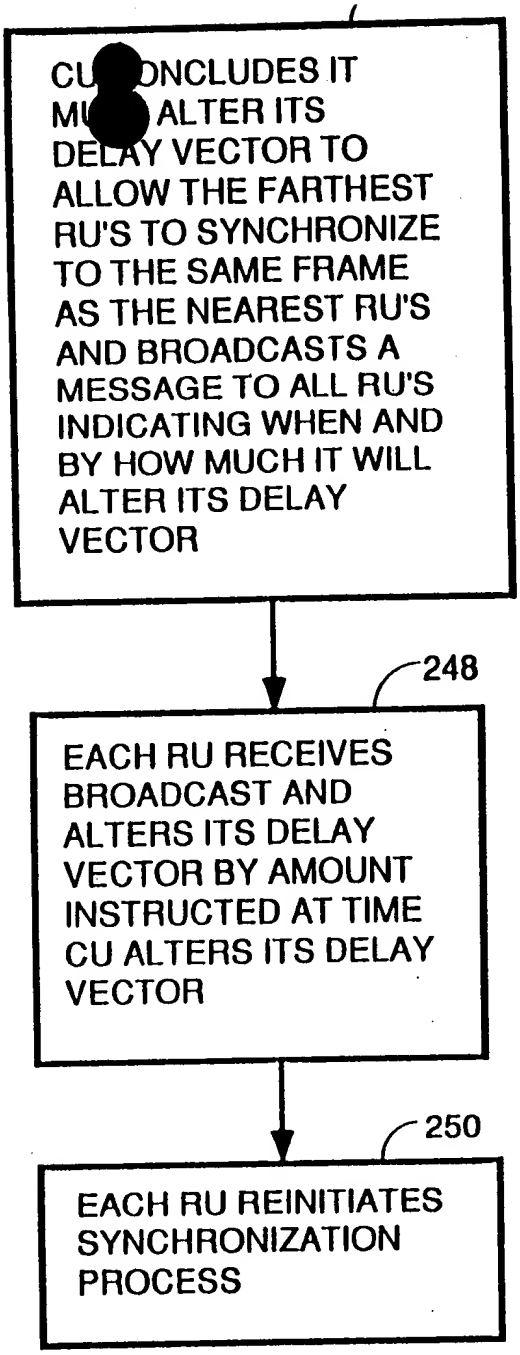


FIG. 9
PRECURSOR EMBODIMENT

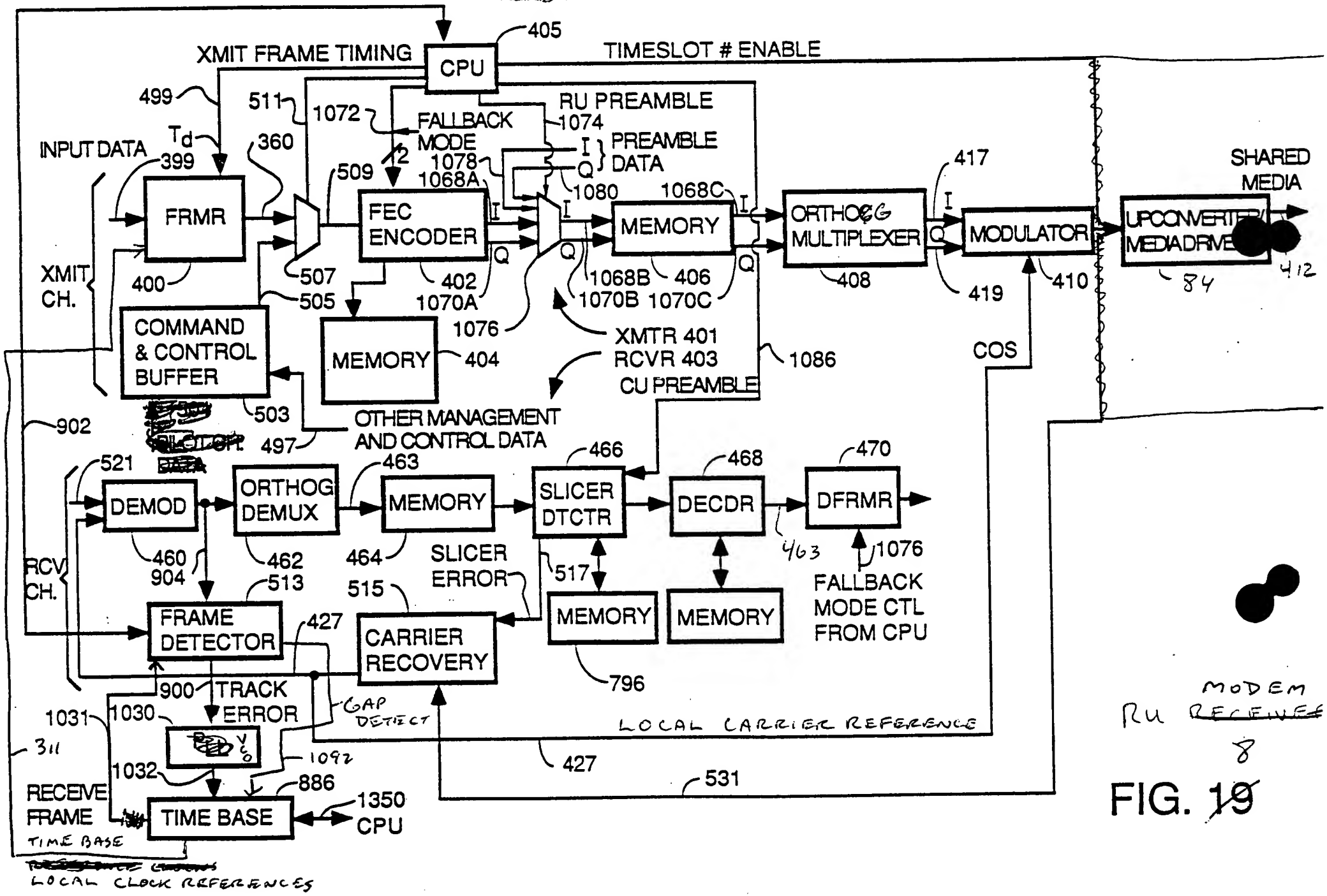

DIGITAL MODEM BLOCK DIAGRAM
XMIT FRAME TIMING
CPU
405
TIMESLOT # ENABLE
499
511
1072
FALLBACK MODE
RU PREAMBLE
1074
PREAMBLE DATA
INPUT DATA
Td
360
399
FRMR
509
12
FEC ENCODER
1078
1068A
1080
1068C
MEMORY
ORTHOG MULTIPLEXER
417
MODULATOR
SHARED MEDIA
UPCONVERTER/ MEDIA DRIVE
412
84
XMIT CH.
400
507
505
402
1070A
1076
1068B
406
1070B 1070C
408
419
410
COMMAND & CONTROL BUFFER
MEMORY
404
XMTR 401
RCVR 403
CU PREAMBLE
1086
COS
902
503
OTHER MANAGEMENT AND CONTROL DATA
497
521
DEMOD
ORTHOG DEMUX
463
MEMORY
466
SLICER DTCTR
468
DECDR
470
DFRMR
460
904
462
464
SLICER ERROR
517
463
1076
RCV CH.
513
515
FRAME DETECTOR
427
CARRIER RECOVERY
MEMORY
MEMORY
FALLBACK MODE CTL FROM CPU
796
900
TRACK ERROR
1031
1030
GAP DETECT
LOCAL CARRIER REFERENCE
311
1092
427
1032
886
531
RECEIVE FRAME
TIME BASE
1350
CPU
TIME BASE
LOCAL CLOCK REFERENCES
MODEM
RU RECEIVE
8

FIG. 19

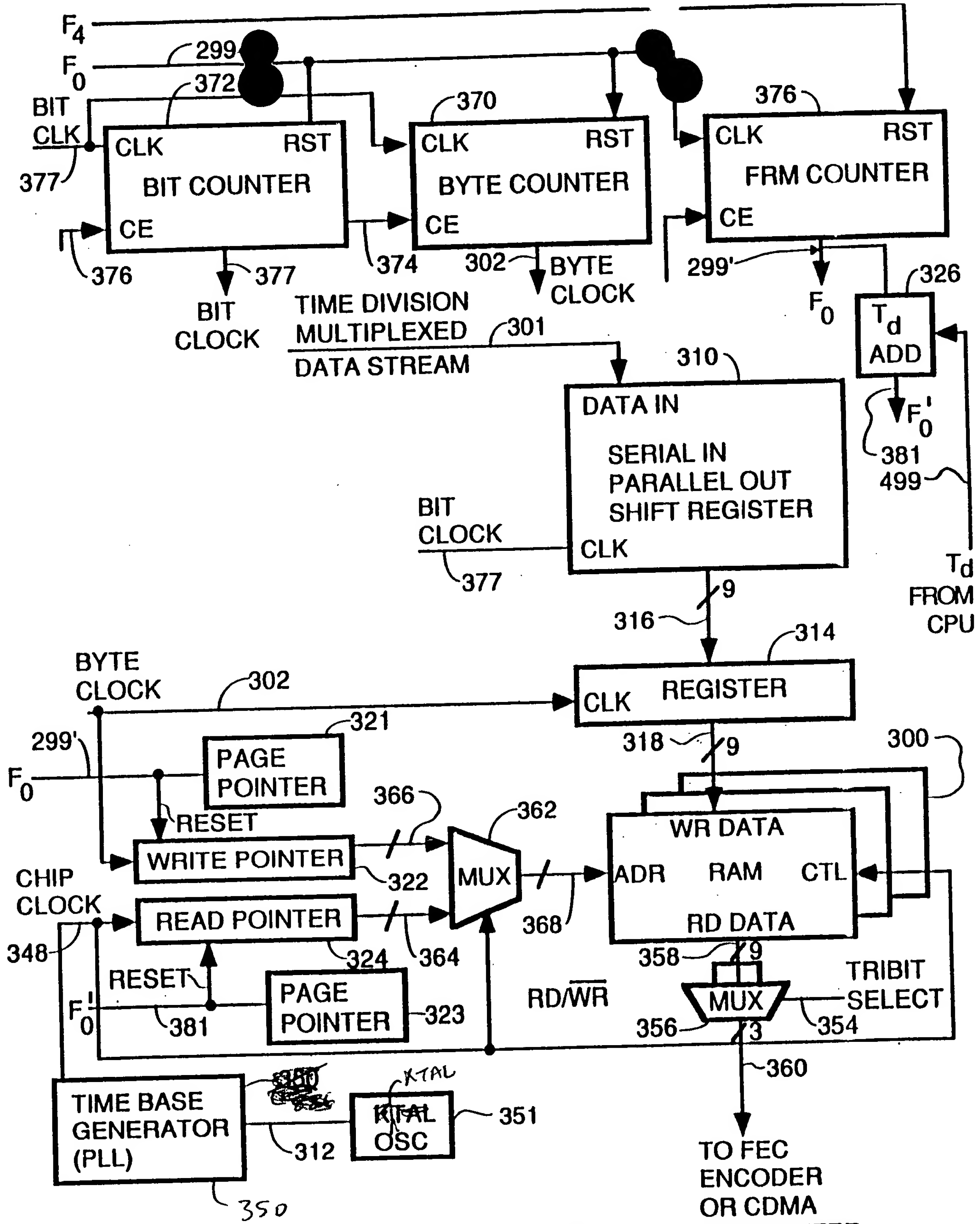

F4
F0
299
372
BIT CLK
377
CLK
RST
BIT COUNTER
CE
376
377
BIT CLOCK
370
BYTE COUNTER
374
302
BYTE CLOCK
376
FRM COUNTER
299'
F0
326
Td ADD
F0'
381
499
Td FROM CPU
TIME DIVISION MULTIPLEXED DATA STREAM
301
310
DATA IN
SERIAL IN PARALLEL OUT SHIFT REGISTER
BIT CLOCK
377
9
316
314
REGISTER
BYTE CLOCK
302
299'
321
PAGE POINTER
F0
RESET
WRITE POINTER
366
322
362
MUX
318
9
300
WR DATA
ADR
RAM
CTL
RD DATA
CHIP CLOCK
348
READ POINTER
324
364
368
RESET
F0'
381
PAGE POINTER
323
RD/WR
358
9
MUX
TRIBIT SELECT
356
3
354
360
TIME BASE GENERATOR (PLL)
312
XTAL OSC
351
350
TO FEC ENCODER OR CDMA MUX/BUFFER

FIG. ~~12~~ 9

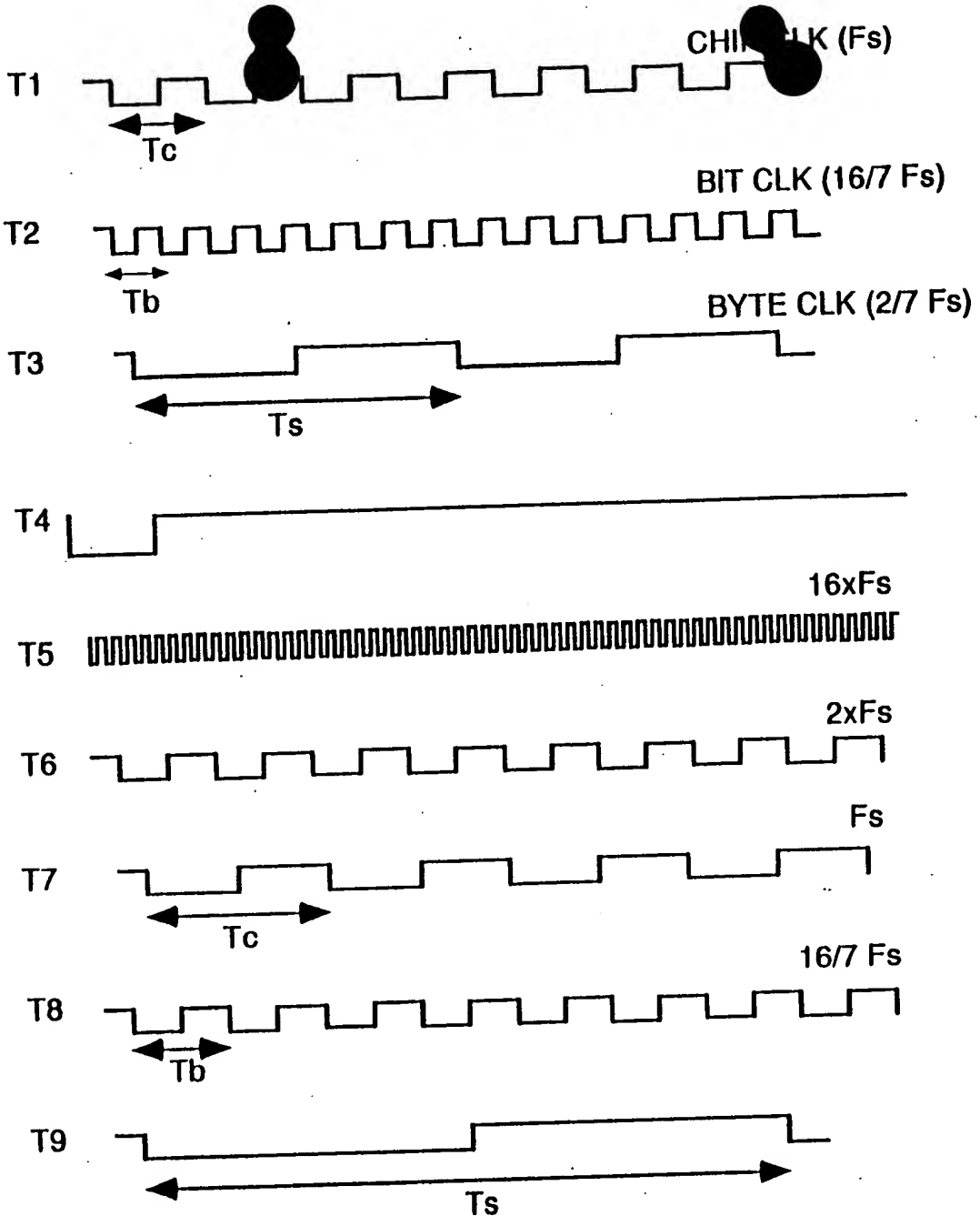
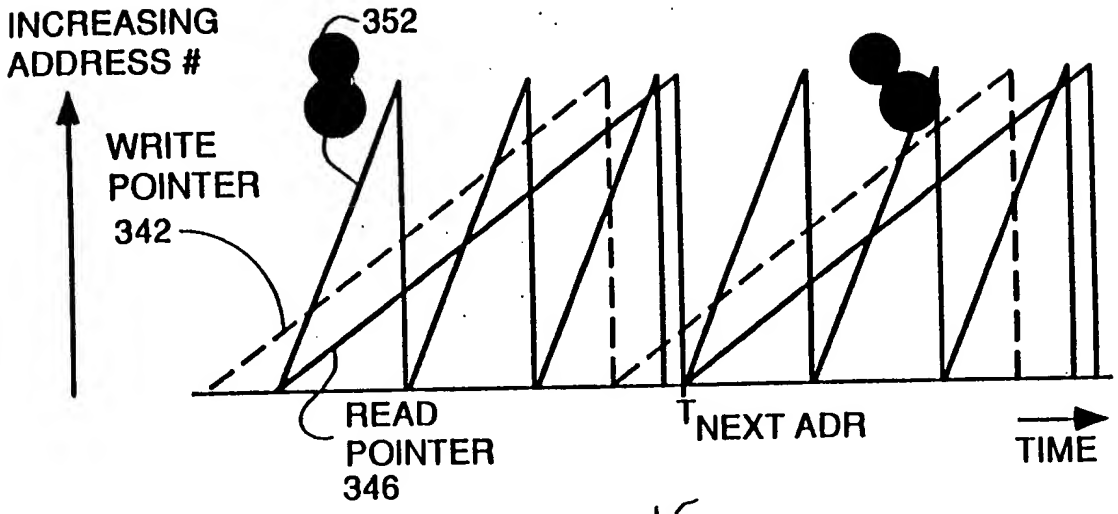
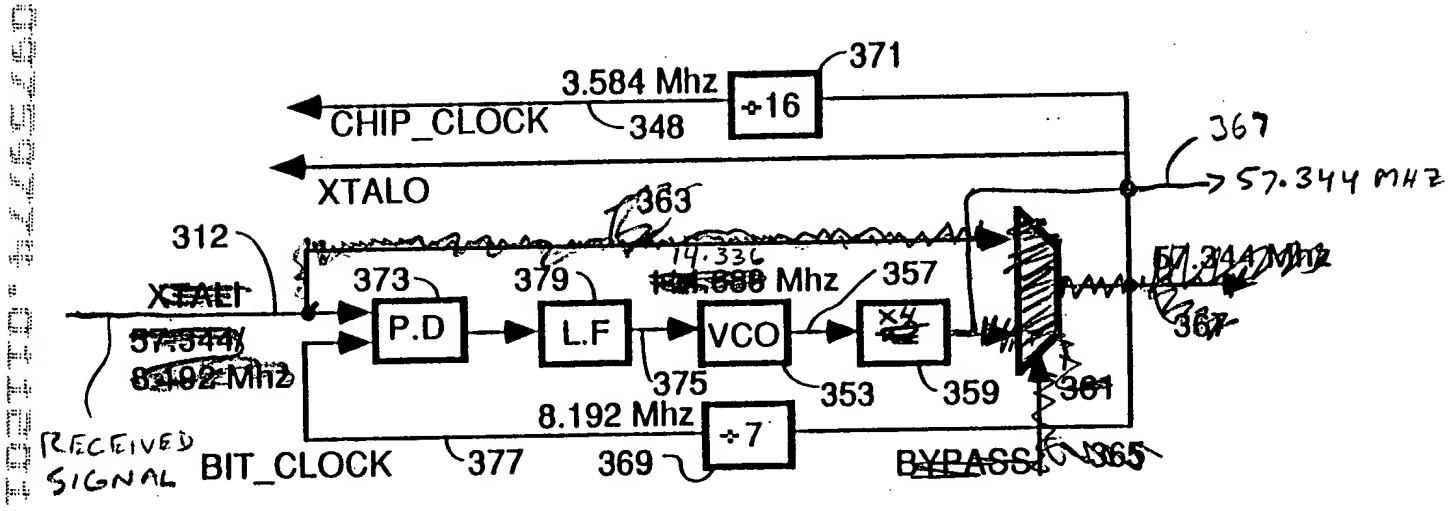

CHI LK (Fs)
T1
Tc
BIT CLK (16/7 Fs)
T2
Tb
BYTE CLK (2/7 Fs)
T3
Ts
T4
16xFs
T5
2xFs
T6
Fs
T7
Tc
16/7 Fs
T8
Tb
T9
Ts

FIG. 10/13



15

FIG. 17



11

FIG. 18

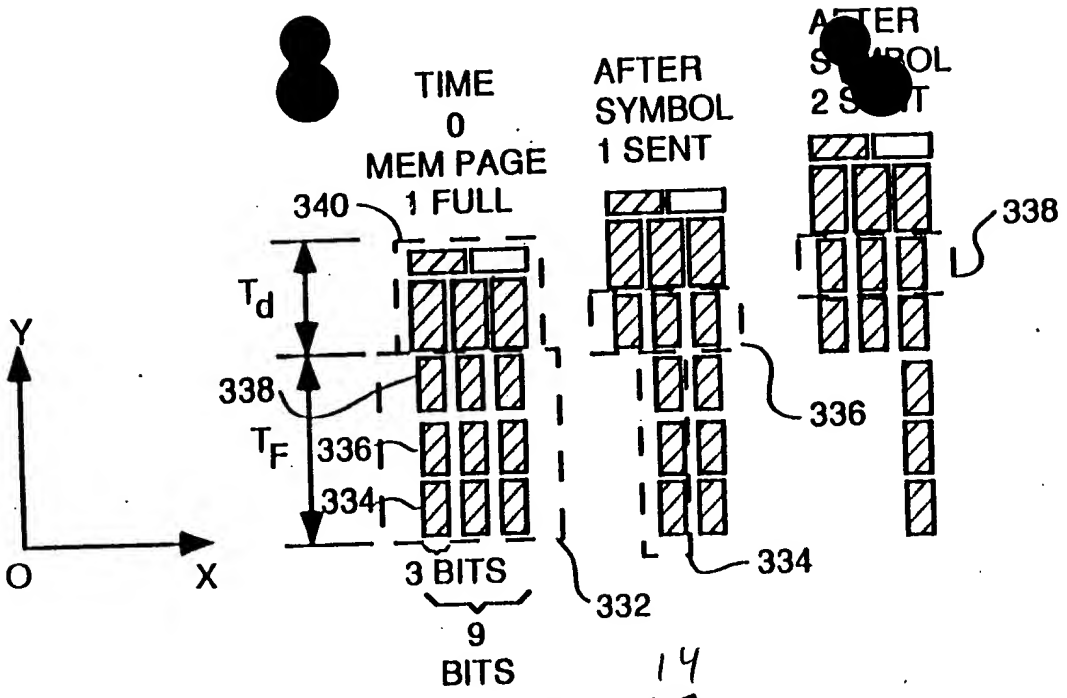


FIG. 14

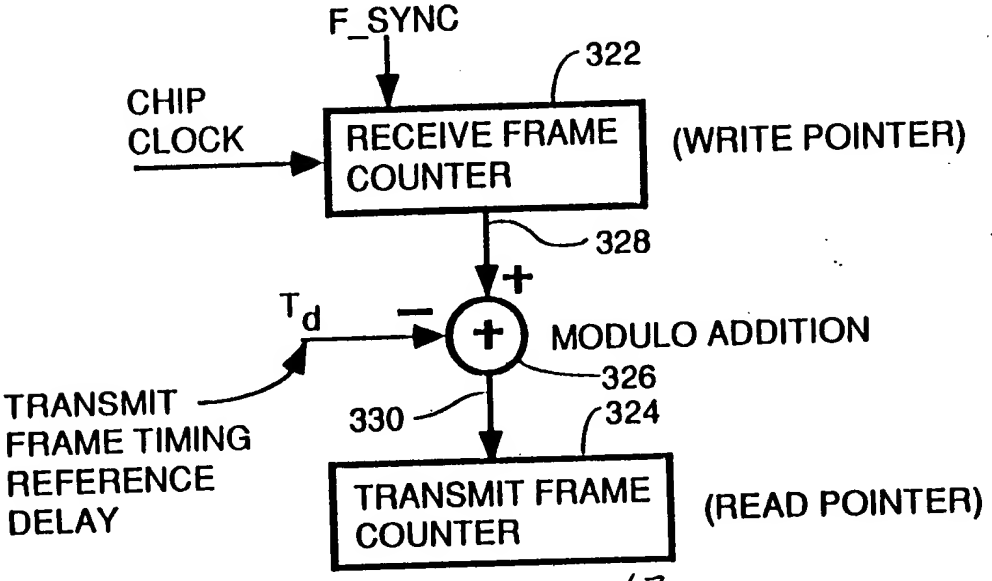


FIG. 15

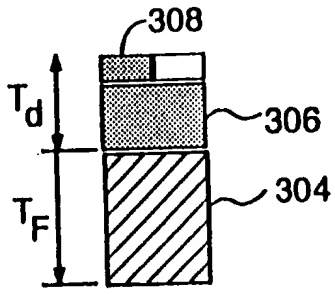


FIG. 16

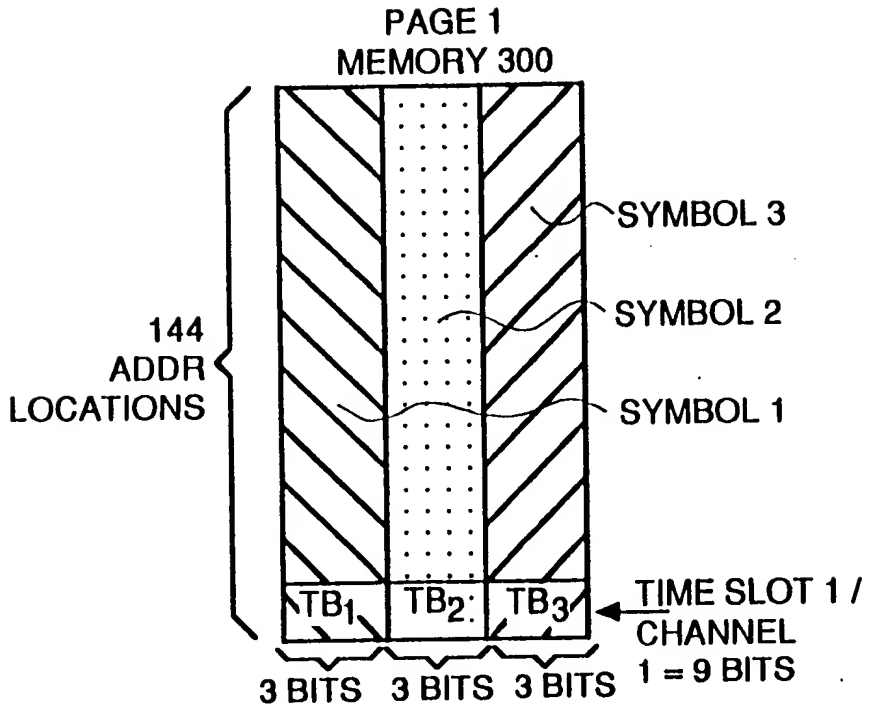
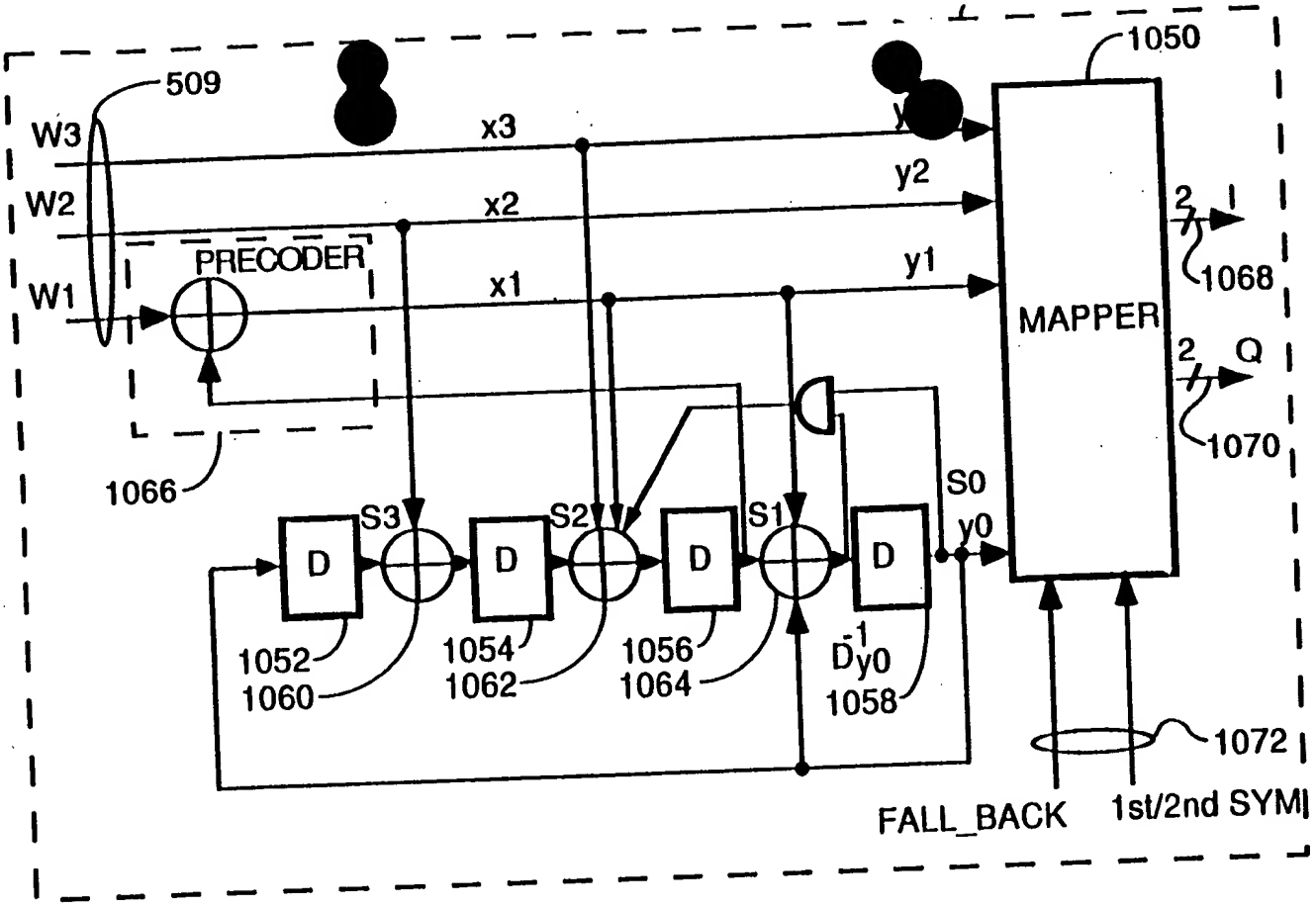

PAGE 1
MEMORY 300
144
ADDR
LOCATIONS
SYMBOL 3
SYMBOL 2
SYMBOL 1
TB1
TB2
TB3
TIME SLOT 1 /
CHANNEL
1 = 9 BITS
3 BITS
3 BITS
3 BITS

FIG. 20

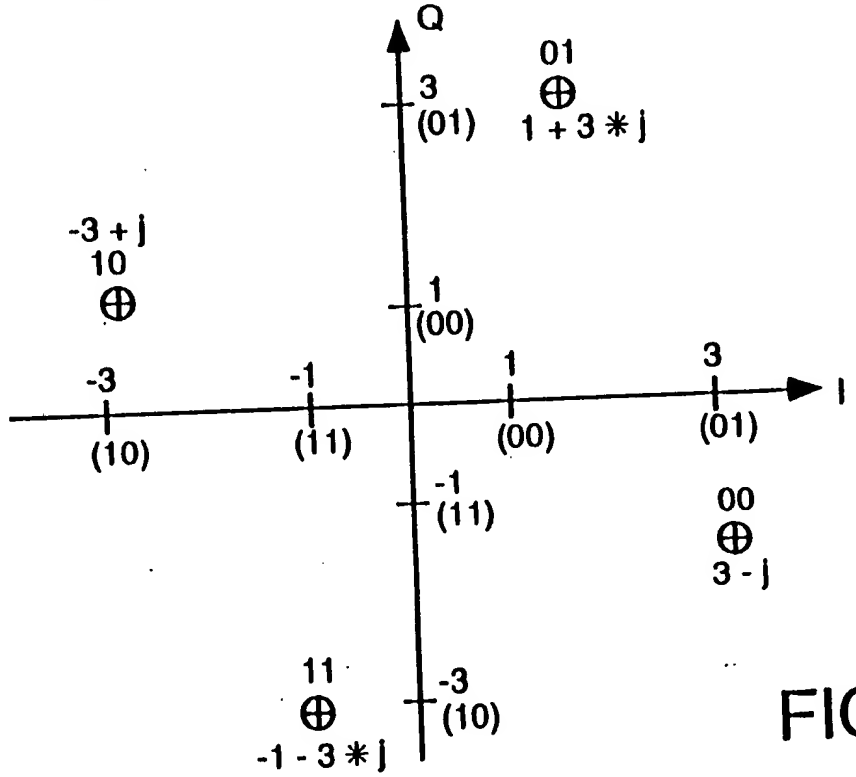


PREFERRED TRELLIS ENCODER

FIG. 42

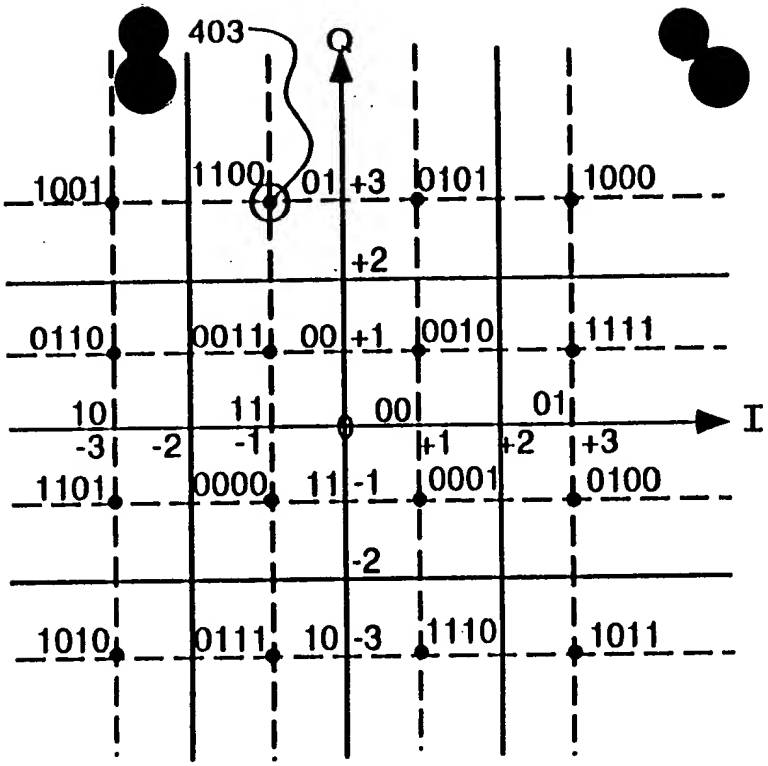
17

MAPPING FOR FALL-BACK MODE - LSB'S



21

FIG. 43



18

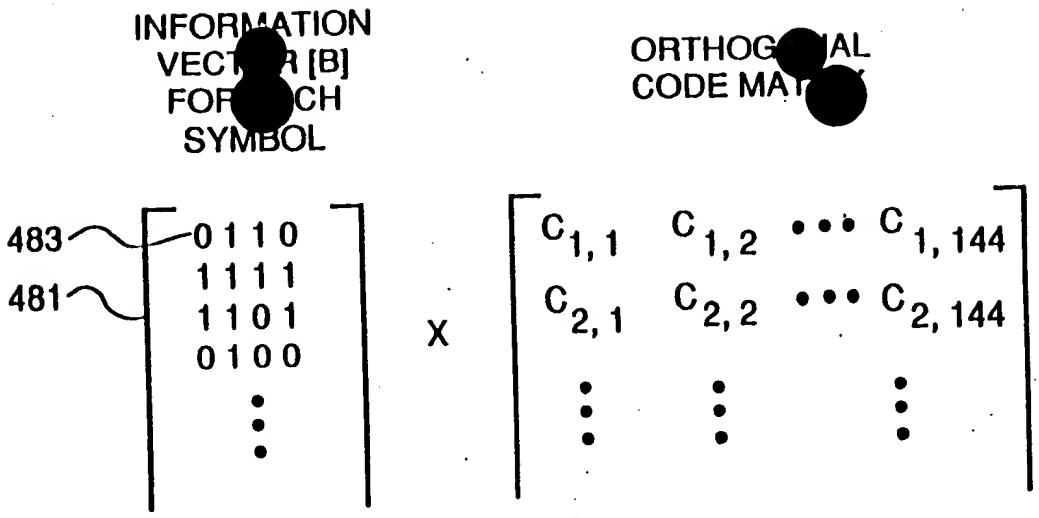
FIG. 21

CODE	INPHASE	QUADRATURE	
0000	111	111	= -1 - j
0001	001	111	= 1 - j
0010	001	001	= 1+ j
0011	111	001	= -1+ j
0100	011	111	= 3 - j
0101	001	011	= 1+ 3* j
0110	101	001	= -3 + j
0111	111	101	= -1 - 3* j
1000	011	011	=+3 + 3* j
1001	101	011	= -3 + 3* j
1010	101	101	= -3 - 3* j
1011	011	101	= 3 - 3* j
1100	111	011	= -1+ 3* j
1101	101	111	= -3 - j
1110	001	101	= 1 - 3* j
1111	011	001	= 3 + j

403

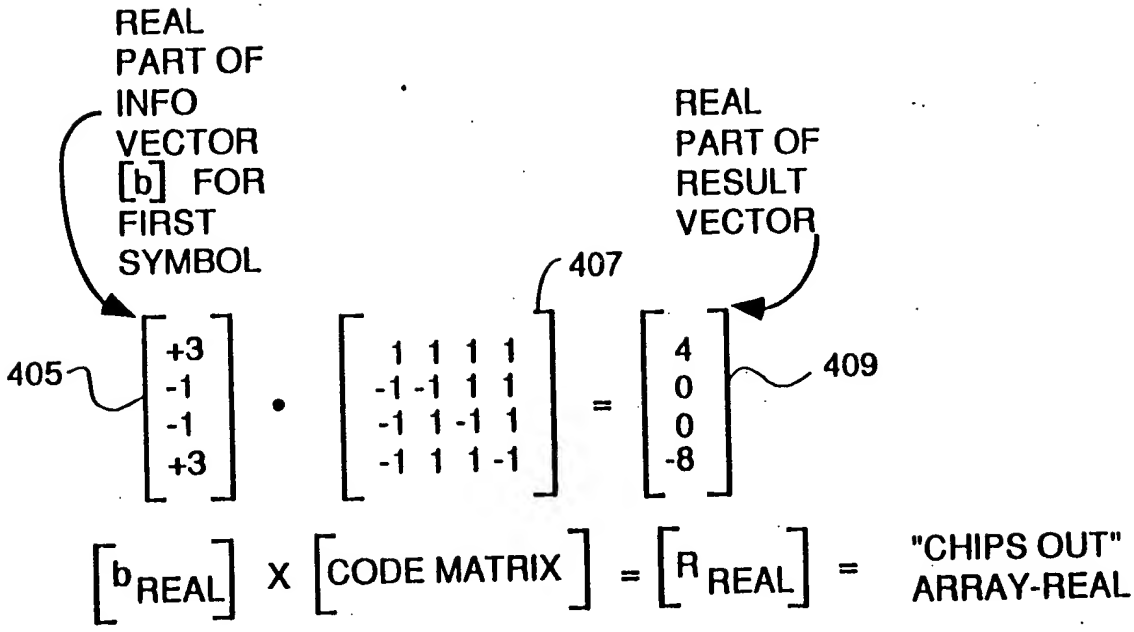
19

FIG. 22



20A

FIG. ~~23~~A



20B

FIG. ~~23~~B

LSBs y1 y0	PHASE	1+jQ
00	0	3-j
01	90	1+j3
10	180	-3+j
11	-90	-1-j3

MSBs y3 y2	PHASE difference (2nd-1st symbol)	1+jQ WHEN LSB=00	1+jQ WHEN LSB=01	1+jQ WHEN LSB=10	1+jQ WHEN LSB=11
00	0	3-j	1+j3	-3+j	-1-j3
01	90	1+j3	-3+j	-1-j3	3-j
10	180	-3+j	-1-j3	3-j	1+j3
11	-90	-1-j3	3-j	1+j3	-3+j

LSB & MSB FALLBACK MODE MAPPINGS

FIG. ~~44~~ 22

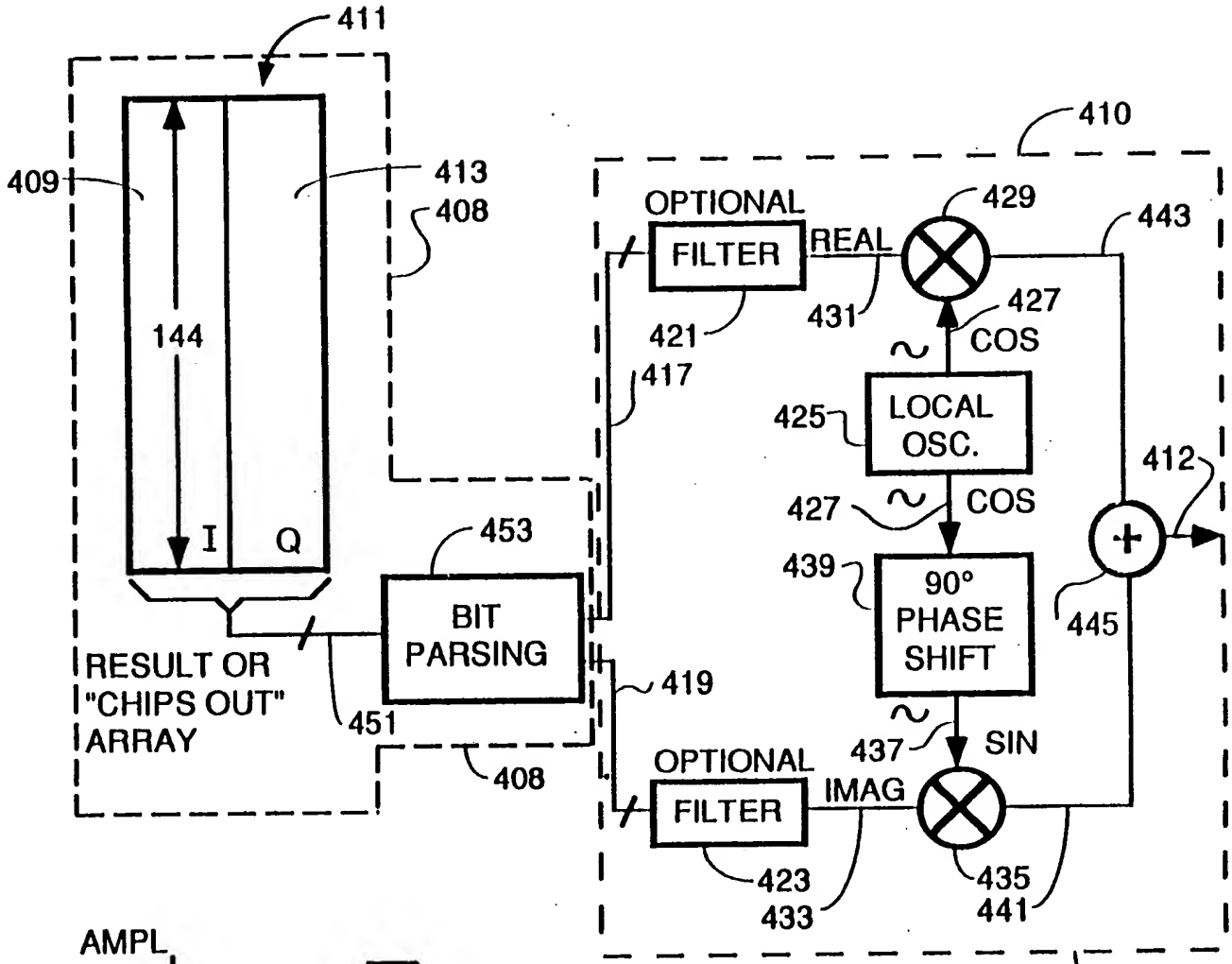

411
409
413
408
144
I
Q
453
BIT PARSING
RESULT OR "CHIPS OUT" ARRAY
451
408
410
OPTIONAL FILTER
REAL
421
431
429
443
427
COS
417
425
LOCAL OSC.
412
427
COS
439
90° PHASE SHIFT
445
419
437
SIN
OPTIONAL FILTER
IMAG
423
433
435
441
410

FIG. 24

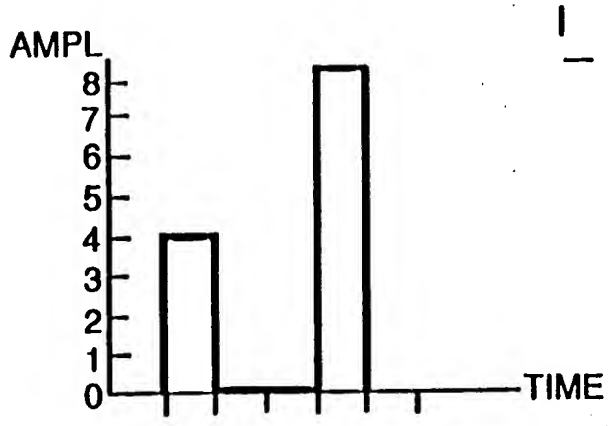
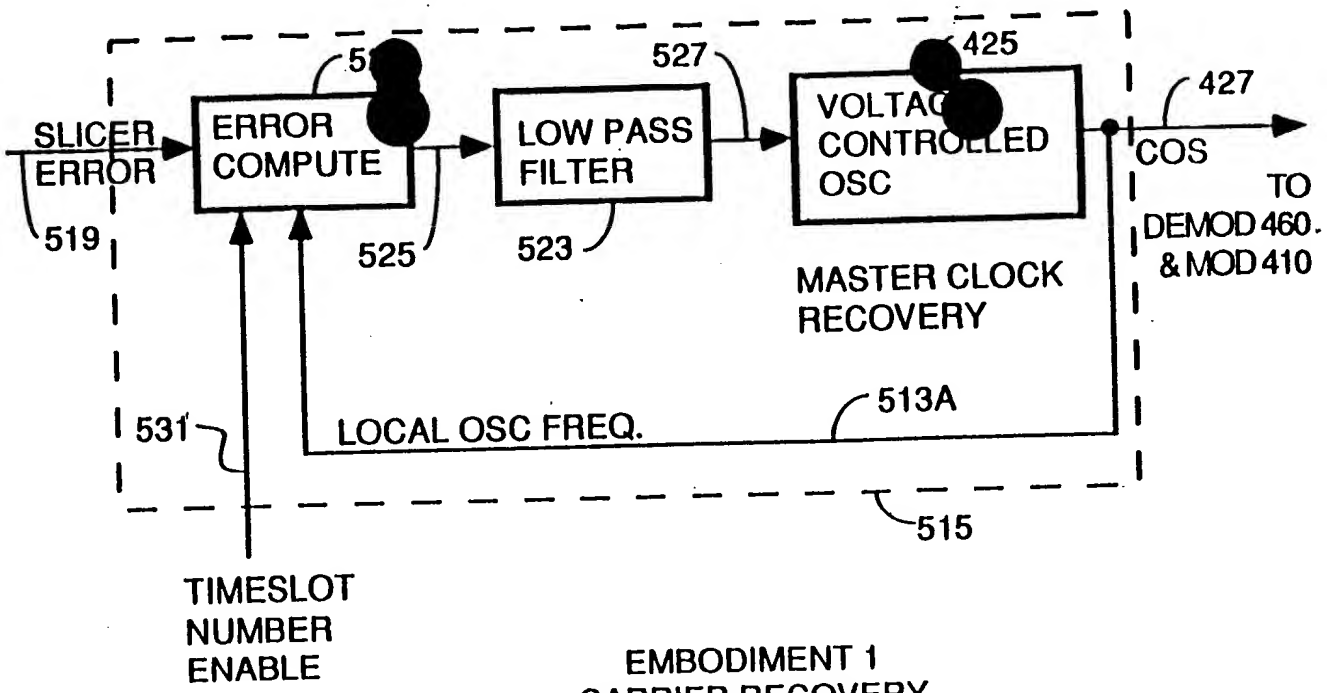

AMPL
8
7
6
5
4
3
2
1
0
TIME

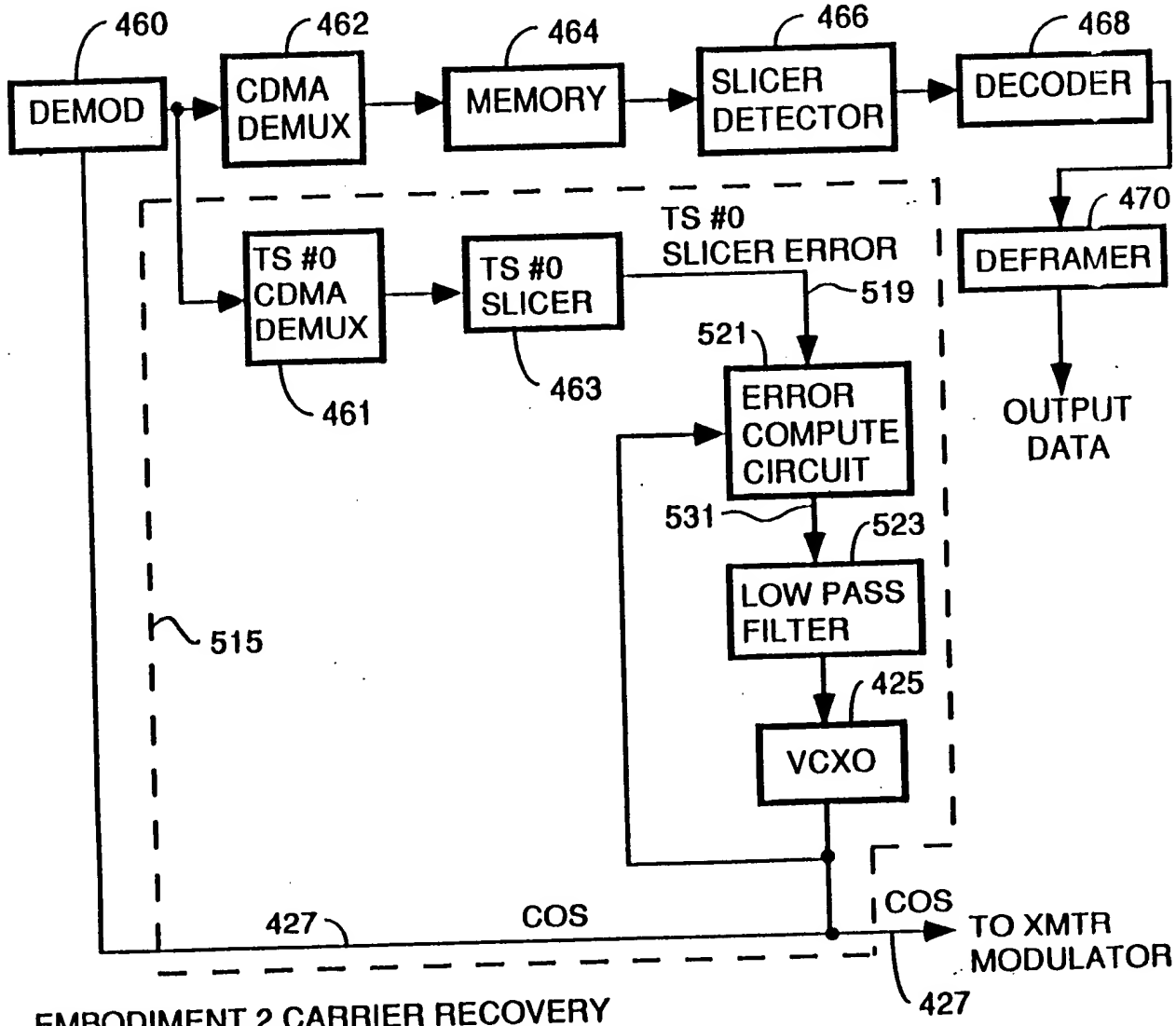
FIG. 25



EMBODIMENT 1
CARRIER RECOVERY

FIG. 35

25



EMBODIMENT 2 CARRIER RECOVERY

FIG. 36

26

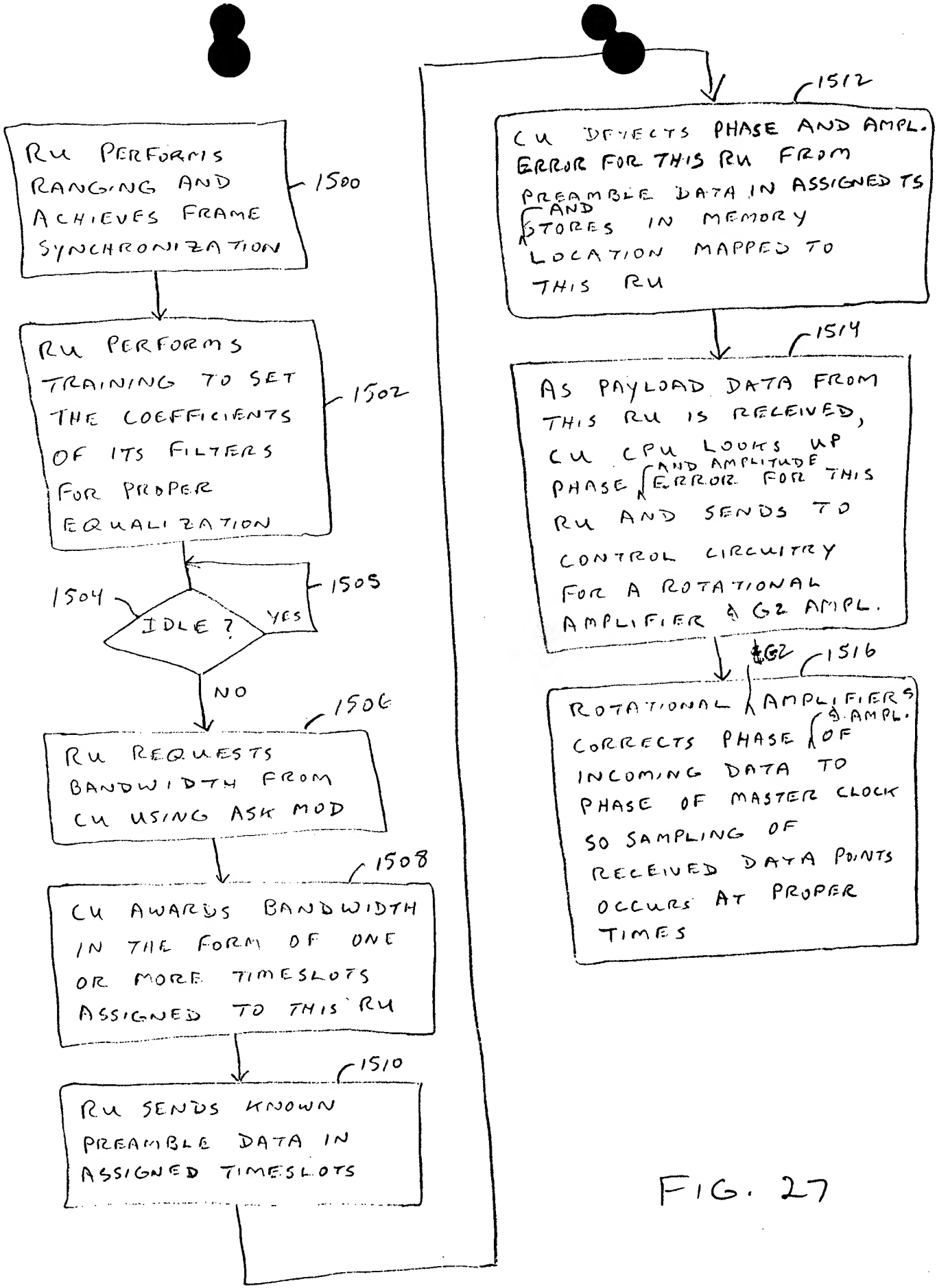
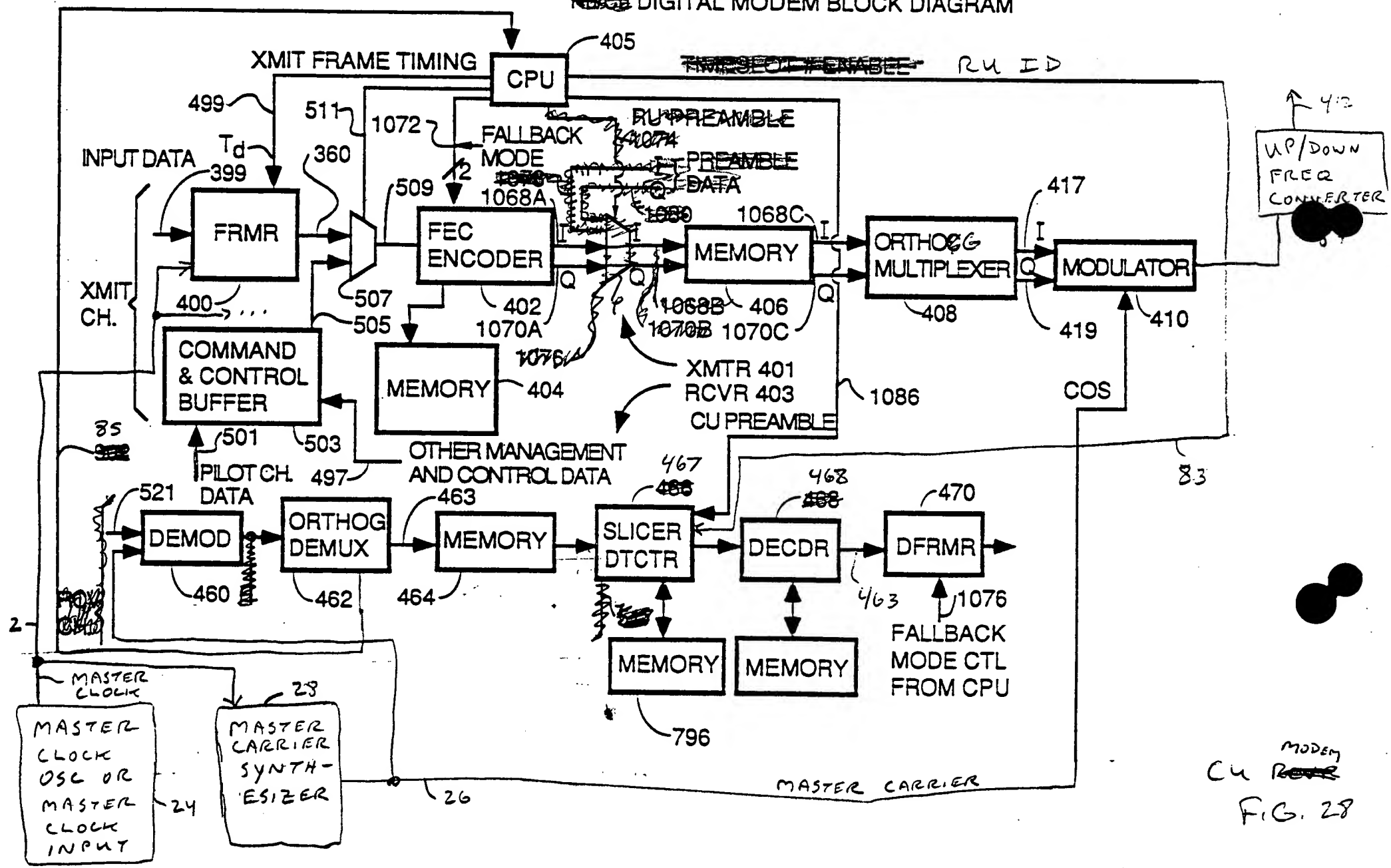

RU PERFORMS RANGING AND ACHIEVES FRAME SYNCHRONIZATION
1500
RU PERFORMS TRAINING TO SET THE COEFFICIENTS OF ITS FILTERS FOR PROPER EQUALIZATION
1502
1504
IDLE ?
YES
1505
NO
RU REQUESTS BANDWIDTH FROM CU USING ASK MOD
1506
CU AWARDS BANDWIDTH IN THE FORM OF ONE OR MORE TIMESLOTS ASSIGNED TO THIS RU
1508
RU SENDS KNOWN PREAMBLE DATA IN ASSIGNED TIMESLOTS
1510
CU DETECTS PHASE AND AMPL. ERROR FOR THIS RU FROM PREAMBLE DATA IN ASSIGNED TS AND STORES IN MEMORY LOCATION MAPPED TO THIS RU
1512
AS PAYLOAD DATA FROM THIS RU IS RECEIVED, CU CPU LOOKS UP PHASE AND AMPLITUDE ERROR FOR THIS RU AND SENDS TO CONTROL CIRCUITRY FOR A ROTATIONAL AMPLIFIER & G2 AMPL.
1514
ROTATIONAL AMPLIFIERS & G2 CORRECTS PHASE OF INCOMING DATA TO PHASE OF MASTER CLOCK SO SAMPLING OF RECEIVED DATA POINTS OCCURS AT PROPER TIMES
1516

FIG. 27



CU MODEM

FIG. 28

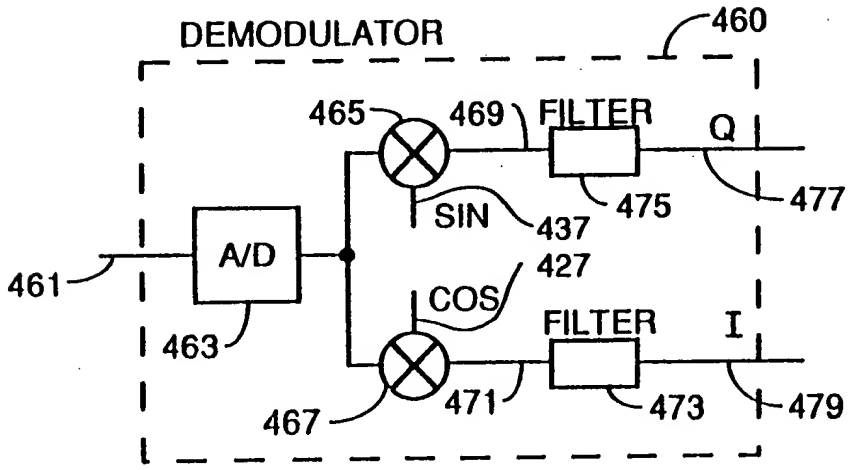

DEMODULATOR
460
465
469
FILTER
Q
475
477
SIN
437
461
A/D
427
COS
FILTER
I
463
467
471
473
479

FIG. 26

29

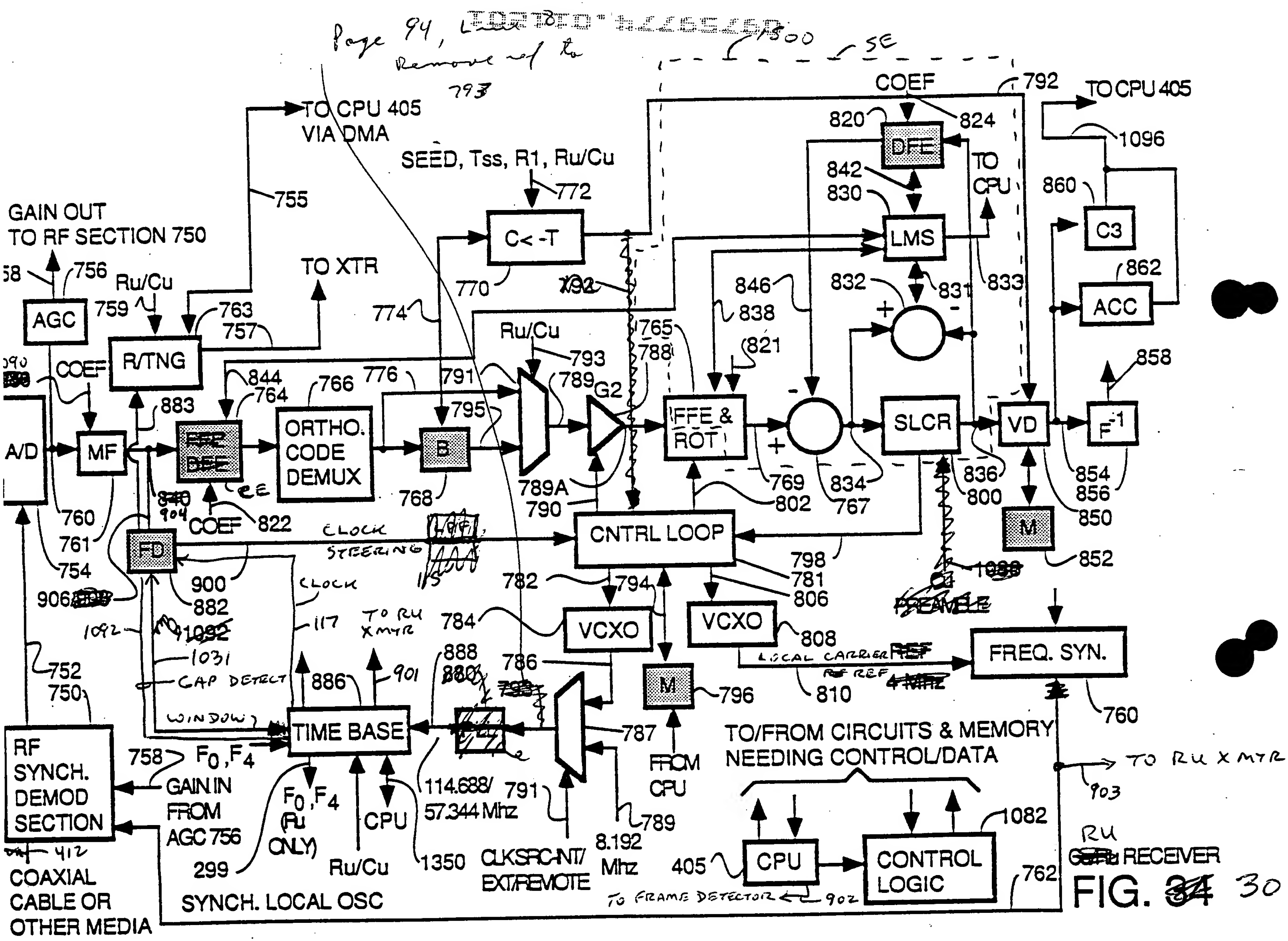

TO CPU 405
VIA DMA
SEED, Tss, R1, Ru/Cu
GAIN OUT
TO RF SECTION 750
AGC
R/TNG
TO XTR
C< -T
COEF
DFE
TO CPU
LMS
C3
ACC
MF
A/D
ORTHO. CODE DEMUX
B
G2
FFE & ROT
SLCR
VD
F^{-1}
CNTRL LOOP
M
FD
VCXO
VCXO
FREQ. SYN.
TIME BASE
FROM CPU
TO/FROM CIRCUITS & MEMORY NEEDING CONTROL/DATA
CPU
CONTROL LOGIC
RF SYNCH. DEMOD SECTION
COAXIAL CABLE OR OTHER MEDIA
SYNCH. LOCAL OSC
GAIN IN FROM AGC 756
F_0, F_4
F_0, F_4 (Ru ONLY)
Ru/Cu
114.688/ 57.344 Mhz
CLKSRC-INT/ EXT/REMOTE
8.192 Mhz
RU RECEIVER

FIG. 30

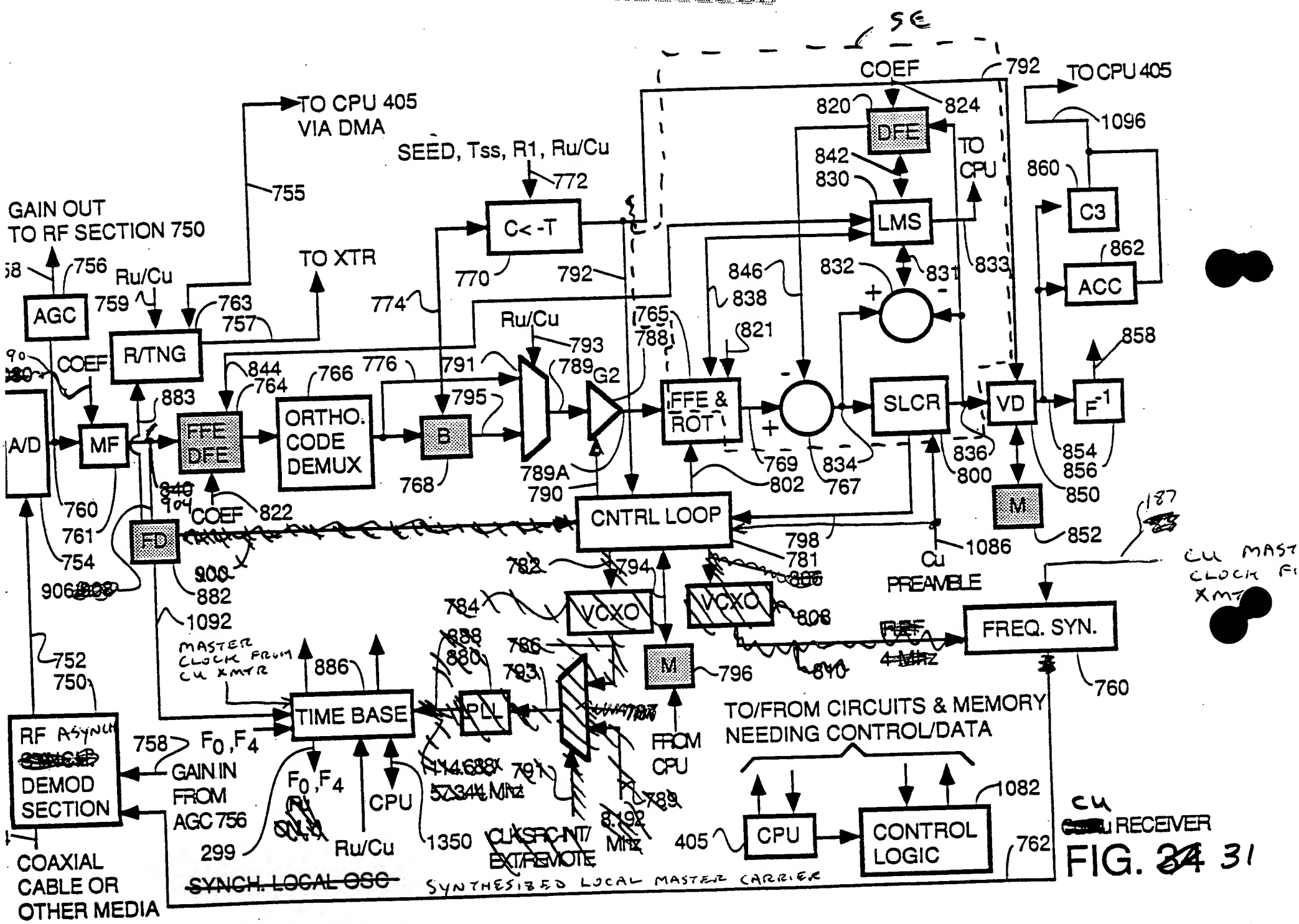

TO CPU 405
VIA DMA
SEED, Tss, R1, Ru/Cu
772
755
GAIN OUT
TO RF SECTION 750
TO XTR
C<-T
770
792
774
Ru/Cu
793
COEF
792
TO CPU 405
820
824
DFE
1096
842
830
TO
CPU
860
C3
LMS
846
838
832
831
833
862
ACC
765
788
821
858
AGC
756
Ru/Cu
759
763
757
R/TNG
776
791
766
844
764
883
795
789
G2
FFE &
ROT
SLCR
VD
F-1
A/D
MF
FFE
DFE
ORTHO.
CODE
DEMUX
B
768
789A
790
769
834
836
800
802
767
854
856
850
760
761
754
840
904
COEF
822
FD
CNTRL LOOP
798
781
782
794
1086
Cu
PREAMBLE
M
852
187
906
882
1092
VCXO
VCXO
784
806
FREQ. SYN.
MASTER
CLOCK FROM
CU XMTR
752
750
886
888
880
786
793
M
796
840
760
TIME BASE
PLL
TO/FROM CIRCUITS & MEMORY
NEEDING CONTROL/DATA
RF ASYNCH
DEMOD
SECTION
758
F0, F4
GAIN IN
FROM
AGC 756
F0, F4
CPU
FROM
CPU
791
789
1082
CU
RECEIVER
299
Ru/Cu
1350
CLKSRC INT/
EXT/REMOTE
8.192
MHz
405
CPU
CONTROL
LOGIC
762
COAXIAL
CABLE OR
OTHER MEDIA
SYNCH. LOCAL OSC
SYNTHESIZED LOCAL MASTER CARRIER

FIG. 24 31

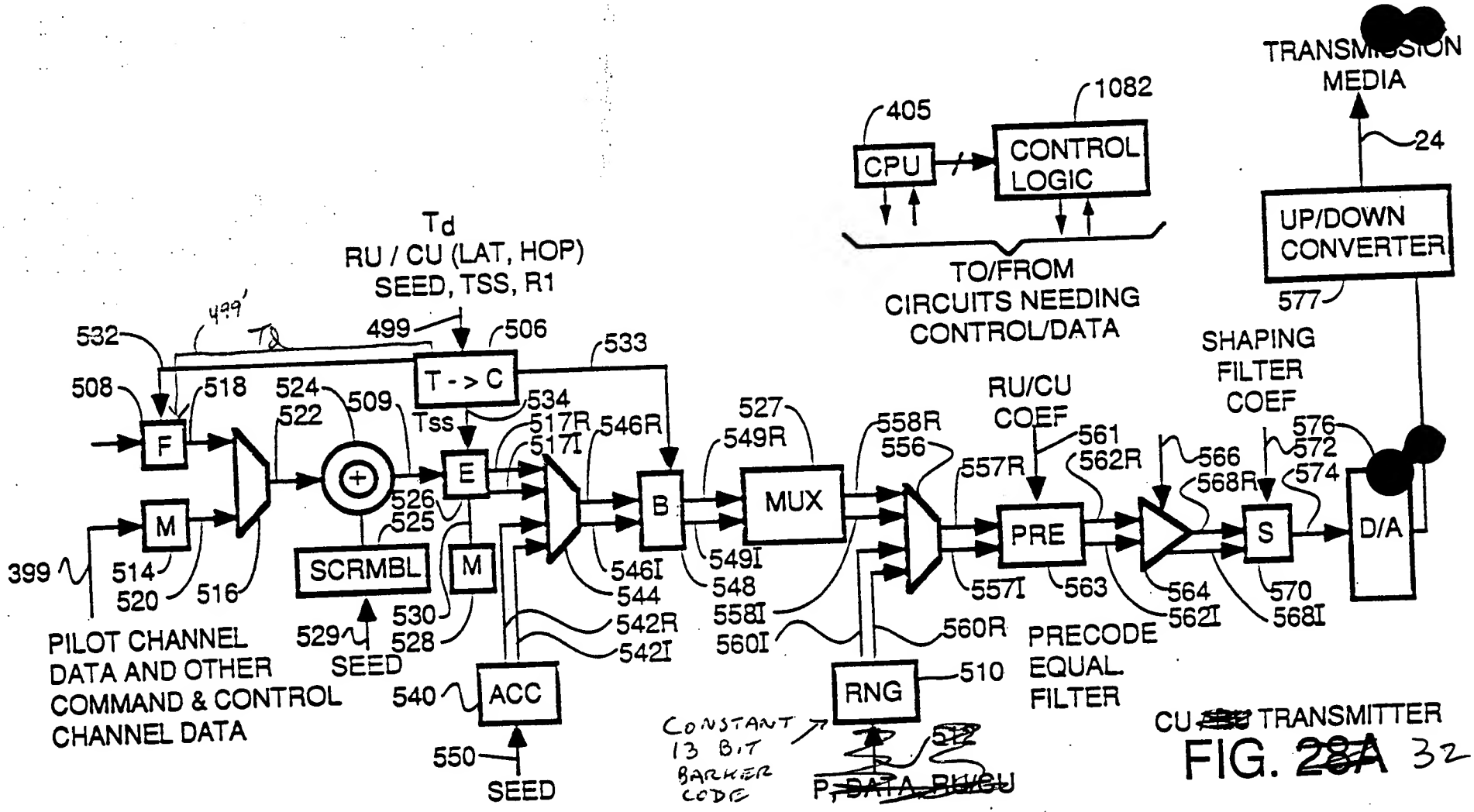

TRANSMISSION MEDIA
24
UP/DOWN CONVERTER
577
1082
405
CPU
CONTROL LOGIC
TO/FROM CIRCUITS NEEDING CONTROL/DATA
Td
RU / CU (LAT, HOP) SEED, TSS, R1
499'
Td
499
506
T -> C
532
533
508
518
524
522
509
534
Tss
517R
517I
546R
527
549R
558R
556
RU/CU COEF
561
562R
557R
SHAPING FILTER COEF
576
572
566
568R
574
F
E
B
MUX
PRE
S
D/A
M
526
525
546I
544
549I
548
558I
560I
557I
563
564
562I
570
568I
399
514
520
516
SCRMBL
M
530
528
529
SEED
542R
542I
560R
PILOT CHANNEL DATA AND OTHER COMMAND & CONTROL CHANNEL DATA
PRECODE EQUAL FILTER
540
ACC
550
SEED
RNG
510
CONSTANT 13 BIT BARKER CODE
512
P-DATA RU/CU
CU TRANSMITTER

FIG. 28A 32

09759778 .012801

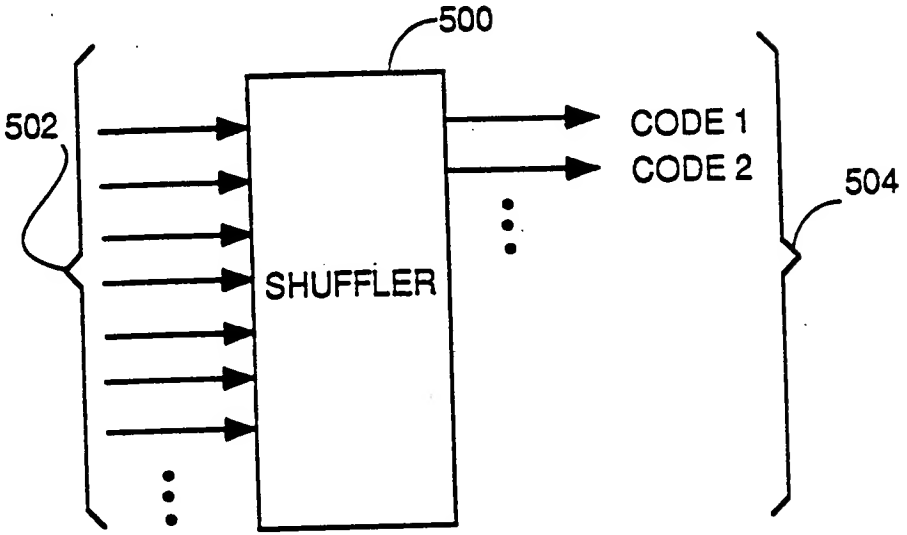


FIG. 27 38

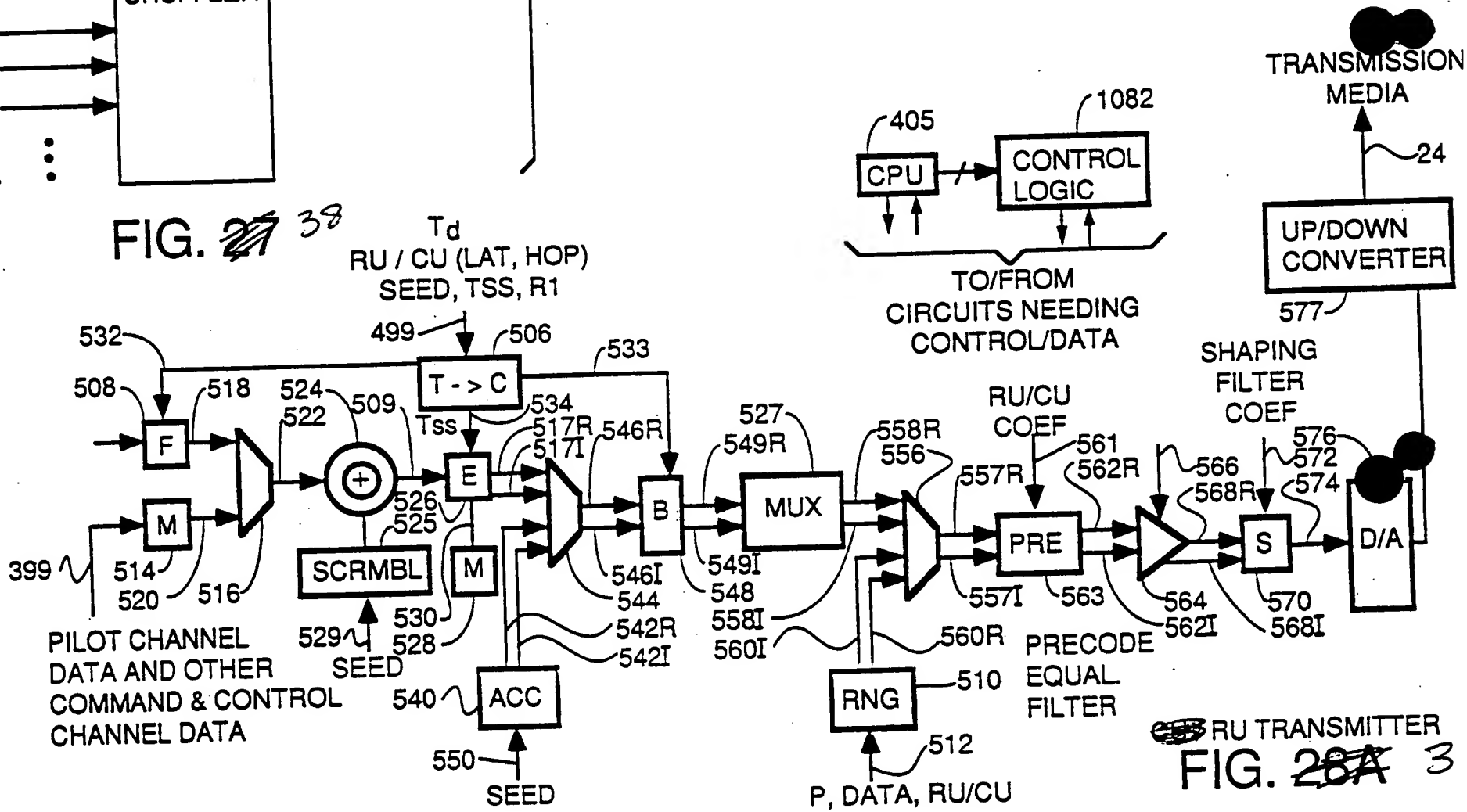
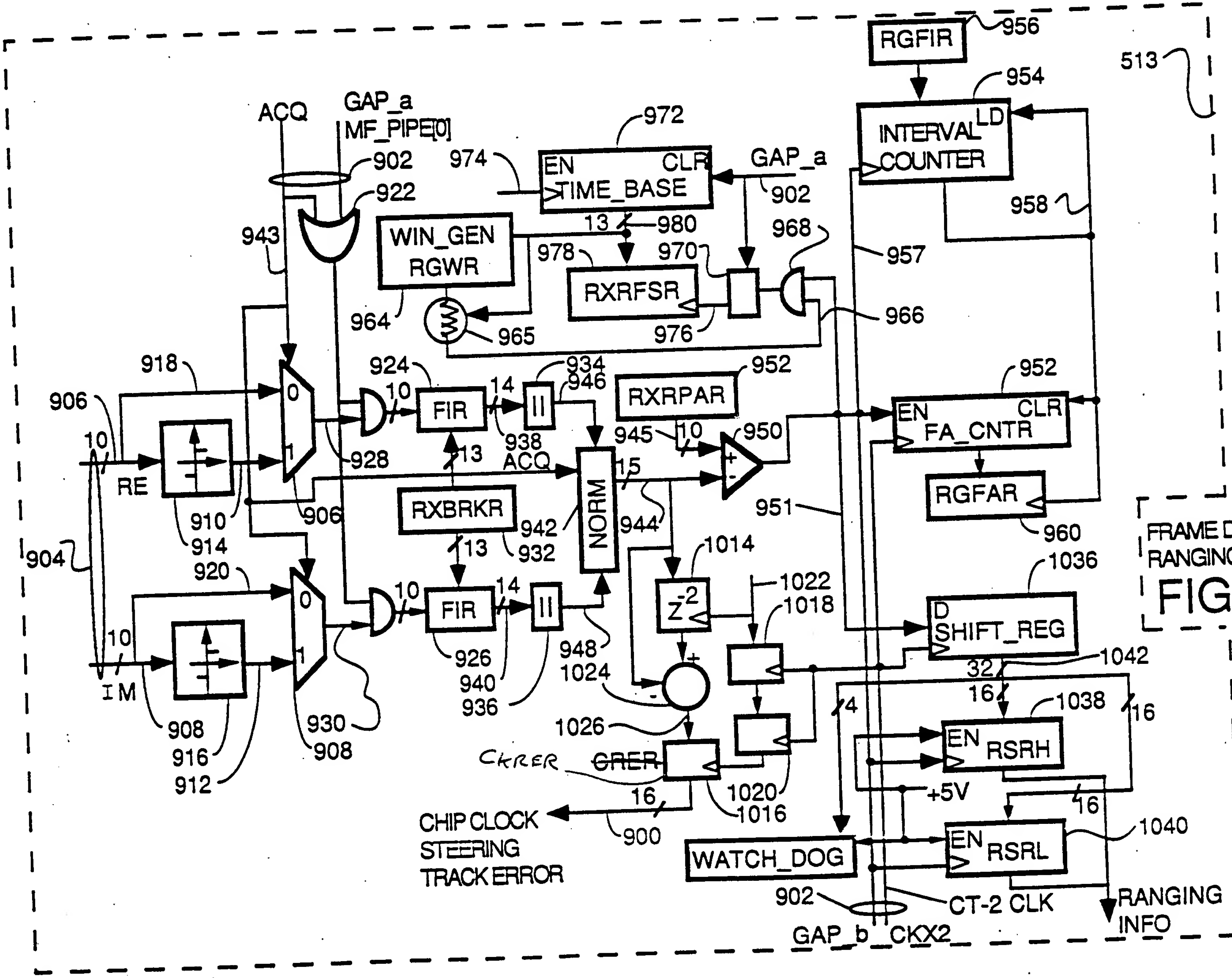


FIG. 28A 3

10311O"h2265260



FRAME DETECTOR/
RANGING DETECTOR

FIG. ~~38~~ 3

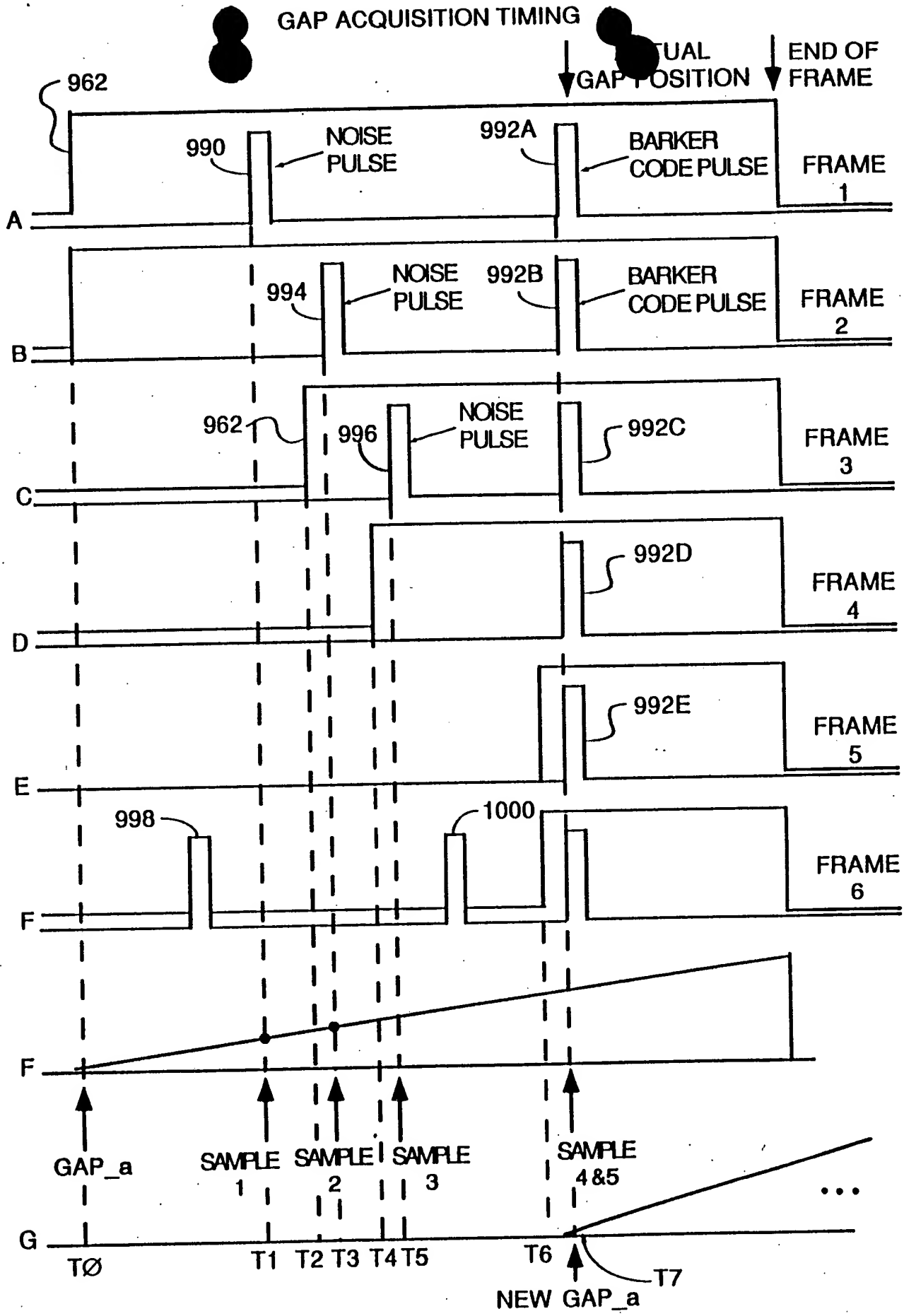
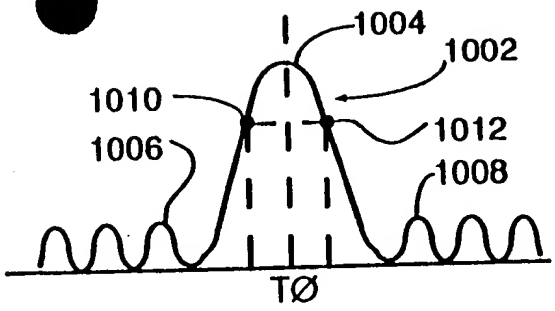
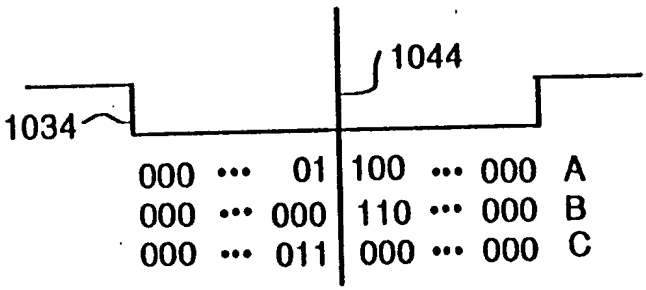

GAP ACQUISITION TIMING
ACTUAL GAP POSITION
END OF FRAME
962
990
NOISE PULSE
992A
BARKER CODE PULSE
FRAME 1
A
994
NOISE PULSE
992B
BARKER CODE PULSE
FRAME 2
B
962
996
NOISE PULSE
992C
FRAME 3
C
992D
FRAME 4
D
992E
FRAME 5
E
998
1000
FRAME 6
F
F
GAP_a
SAMPLE 1
SAMPLE 2
SAMPLE 3
SAMPLE 4&5
G
TØ
T1 T2 T3 T4 T5
T6
T7
NEW GAP_a

FIG. 39 35



36

FIG. 40



37

FIG. 41

FINE TUNING TO CENTER BARKER CODE

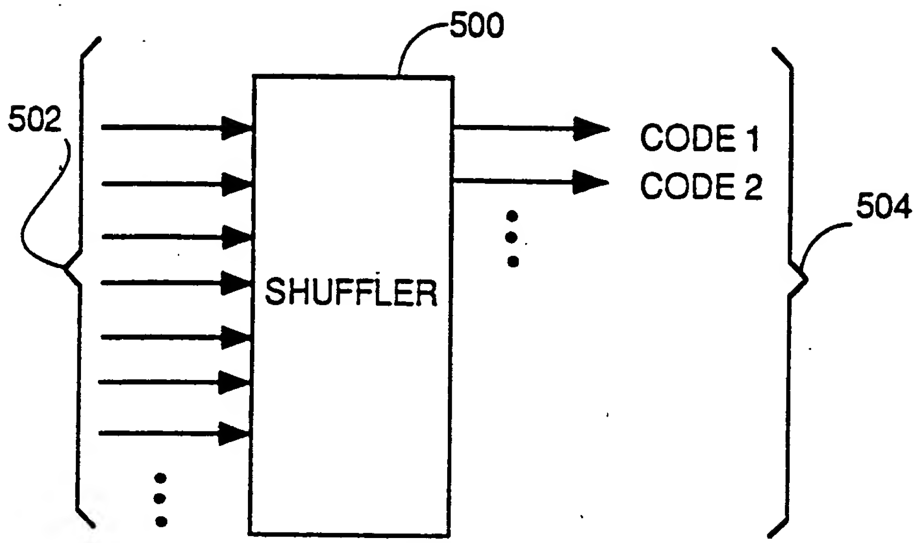


FIG. ~~27~~ 38

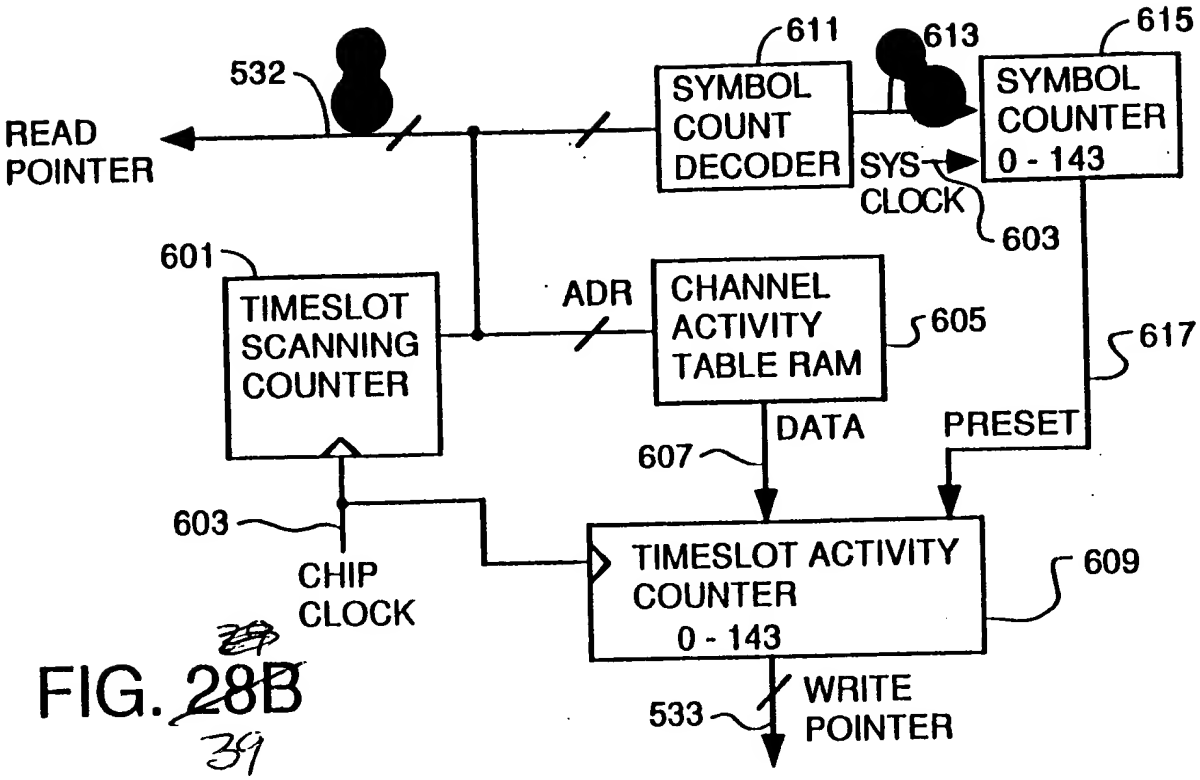


FIG. 28B

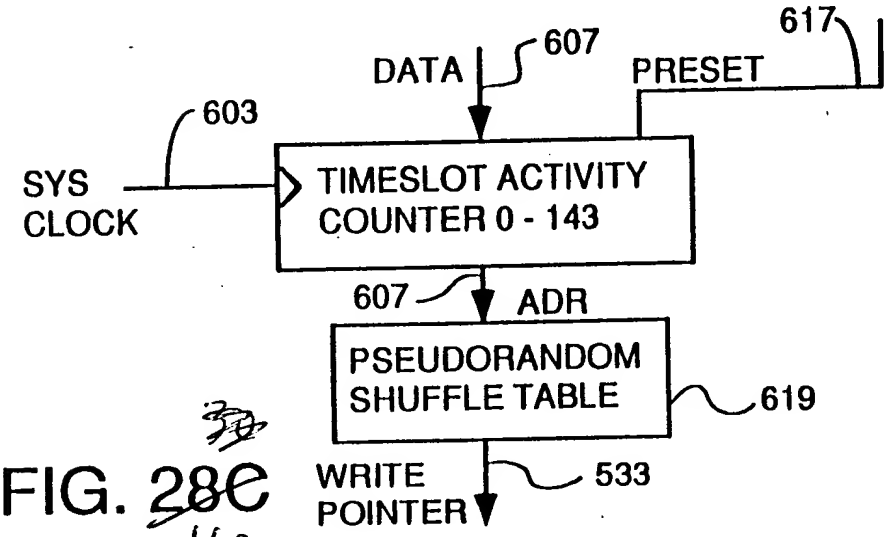


FIG. 28C

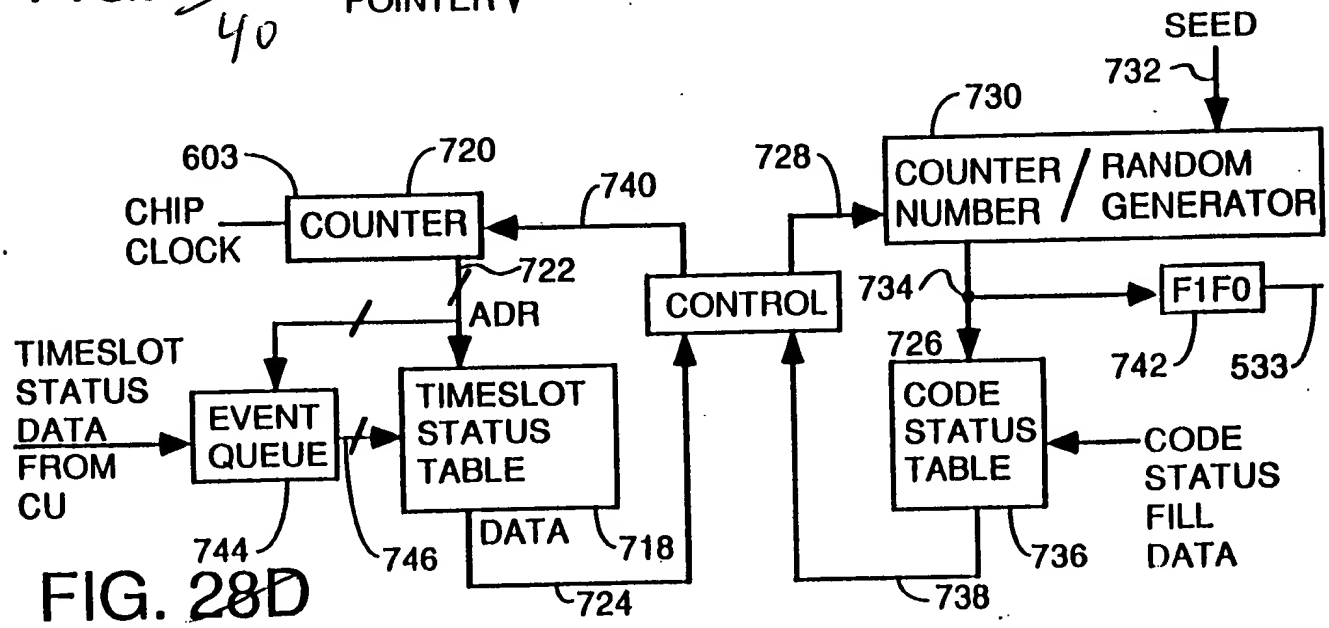
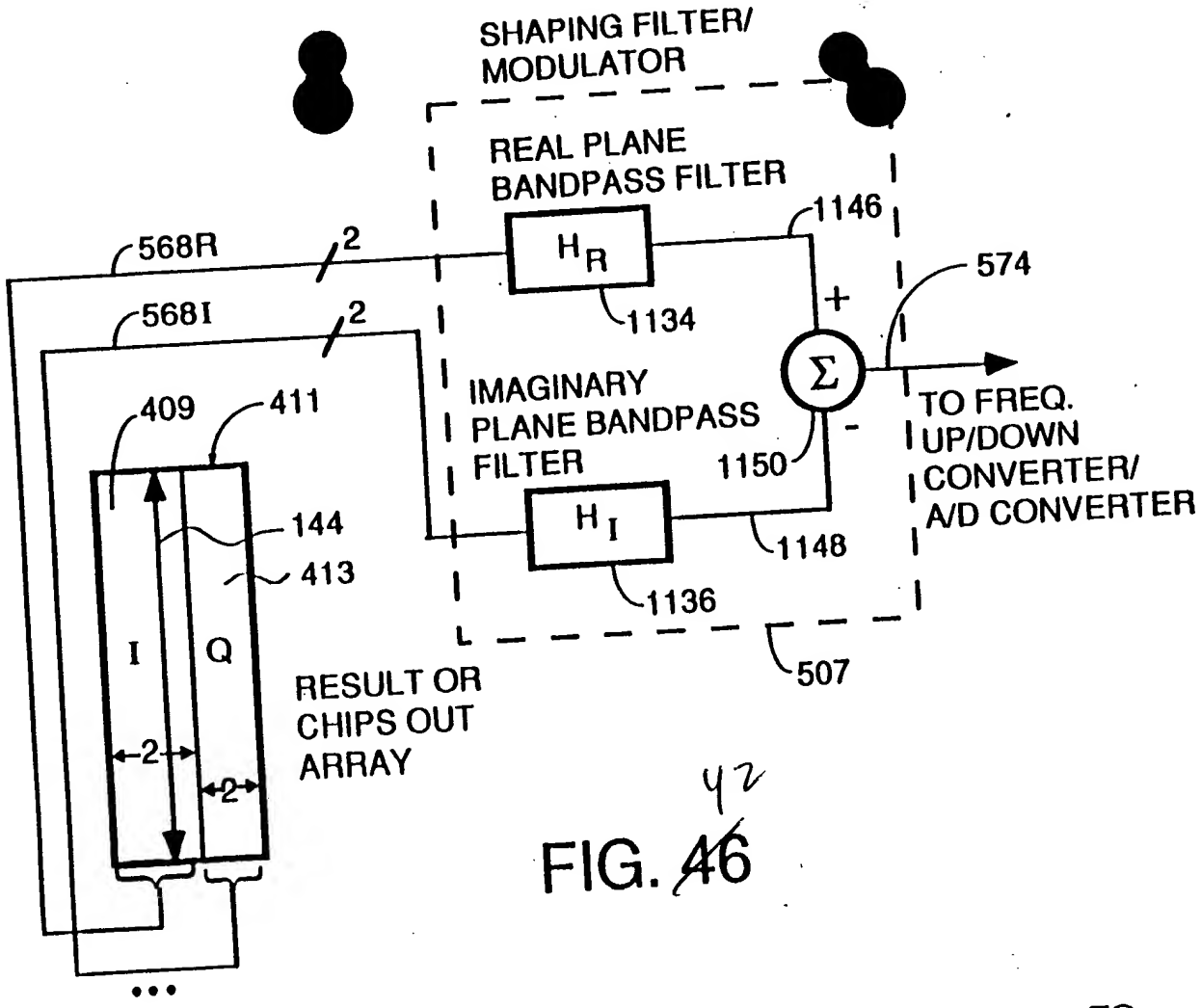
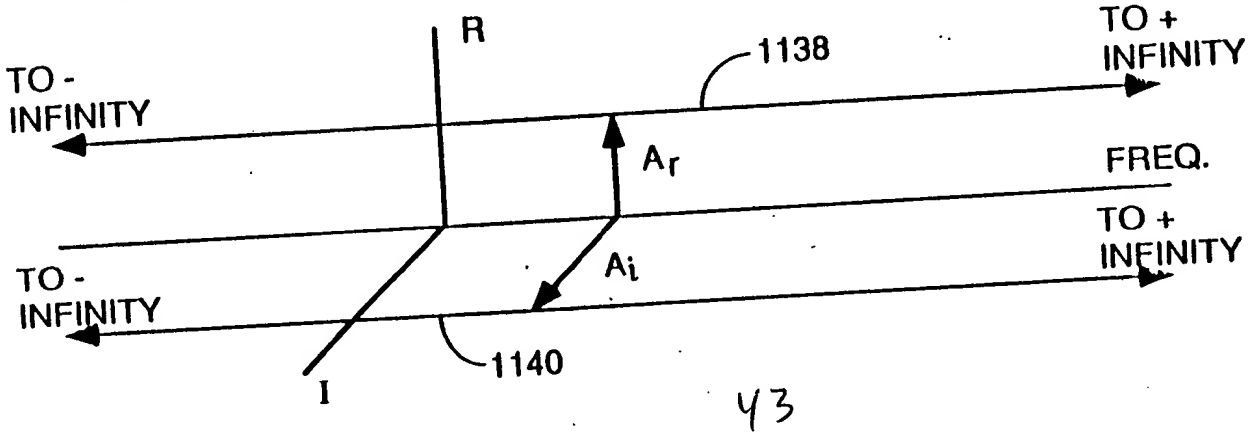


FIG. 28D



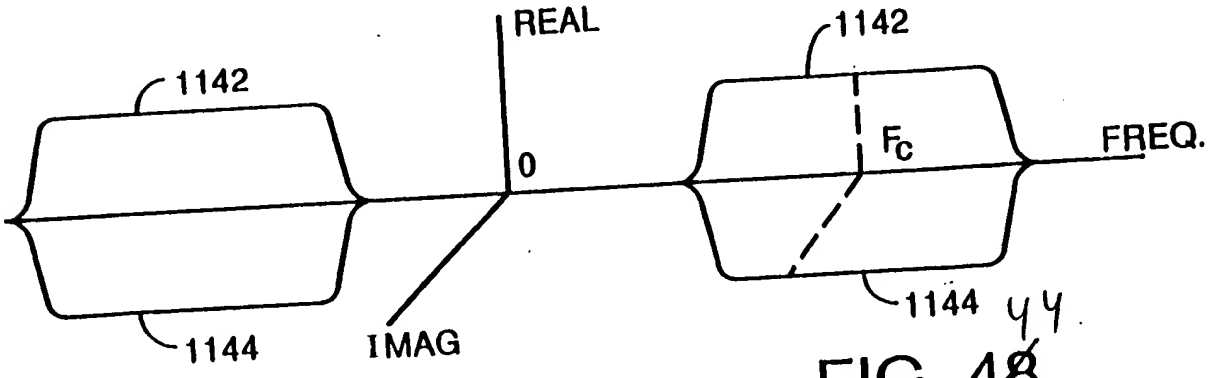
42

FIG. 46



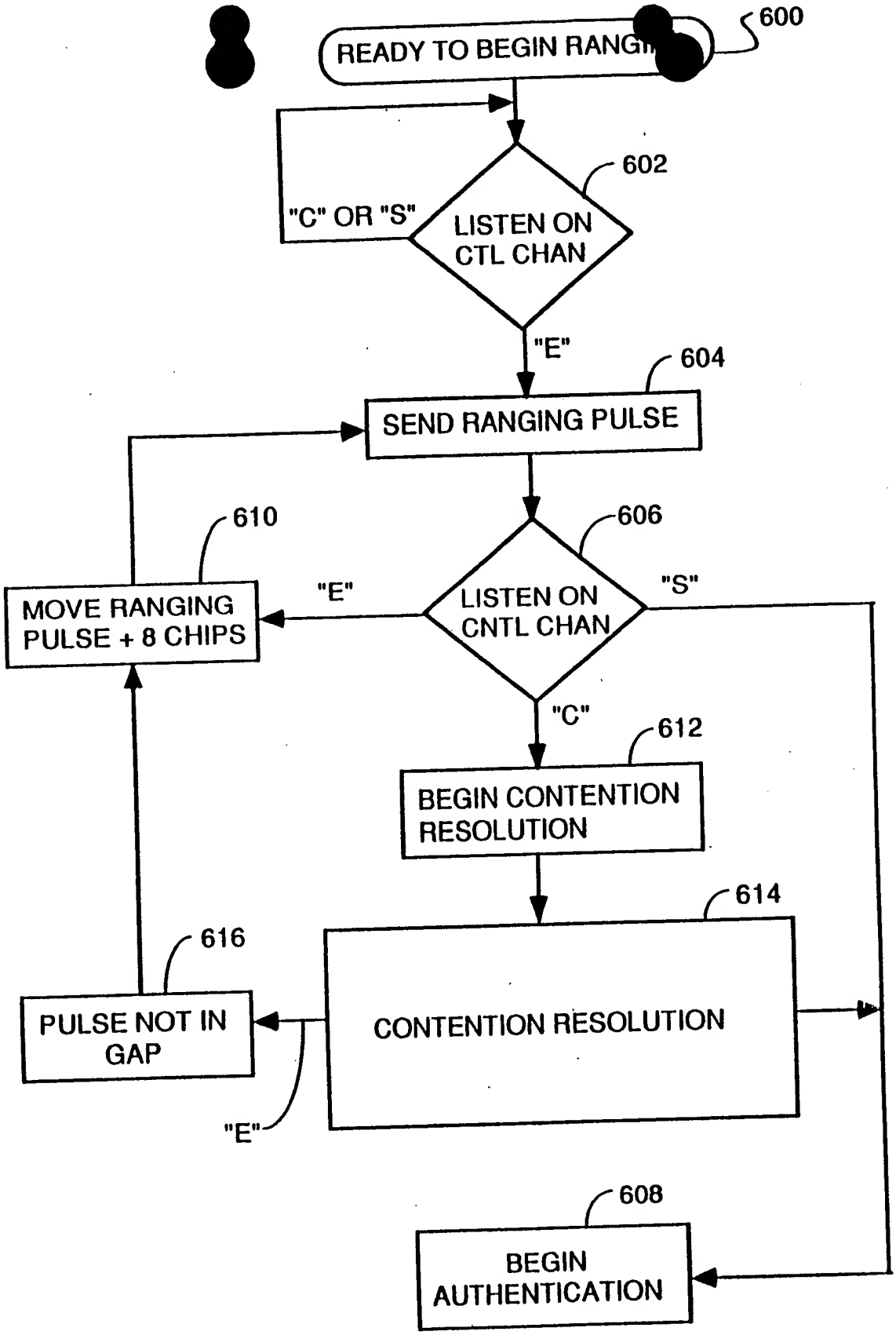
43

FIG. 47



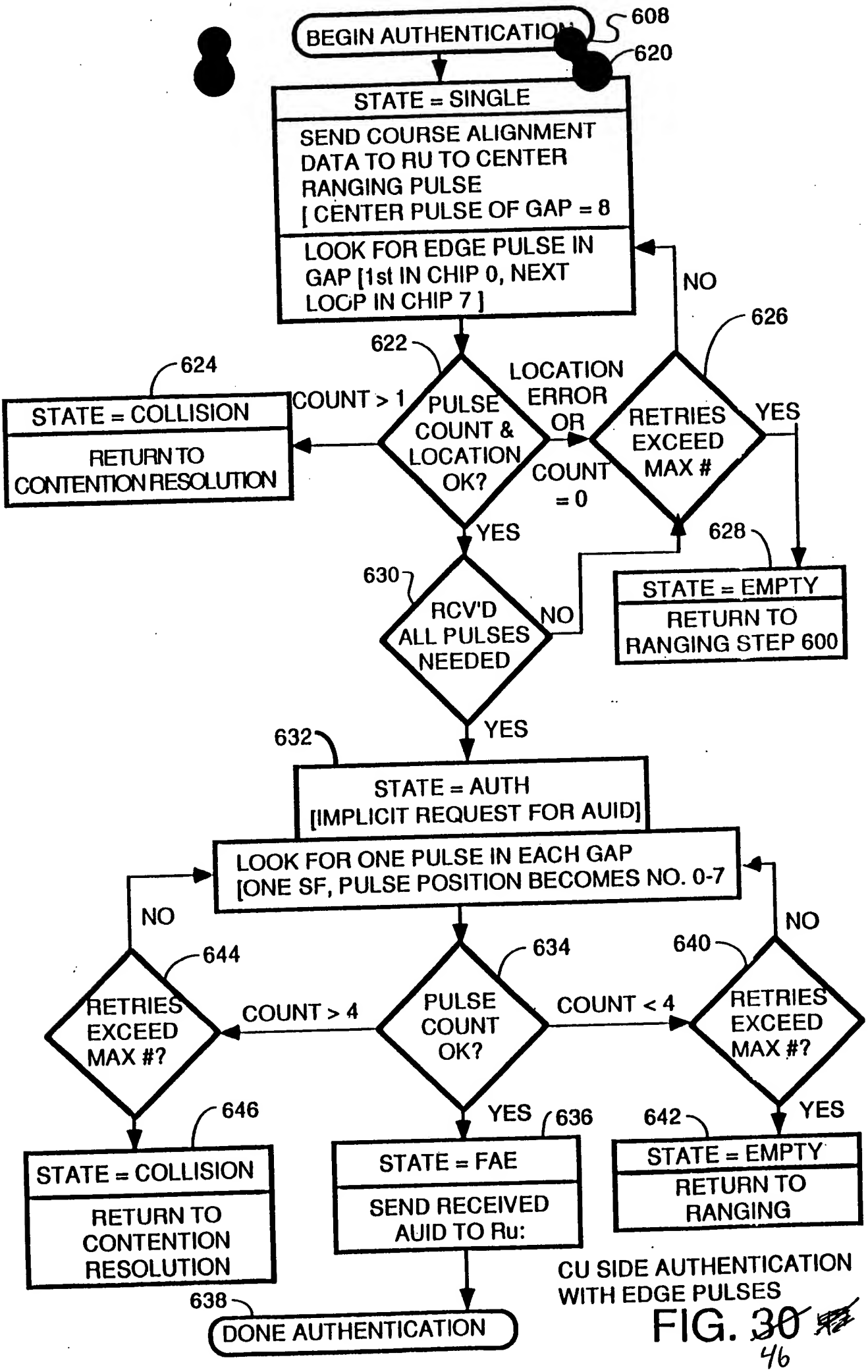
44

FIG. 48



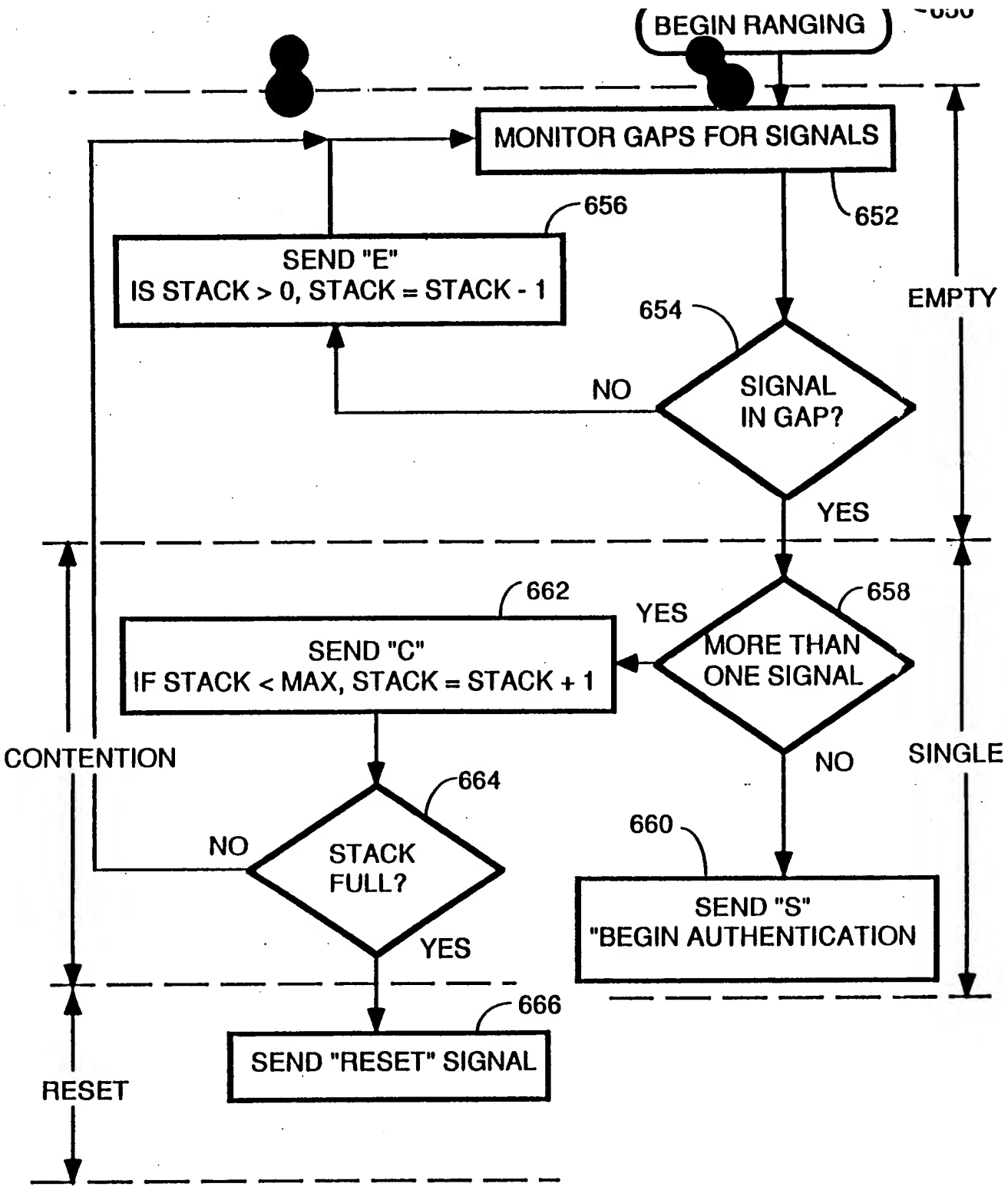
RU RANGING

FIG. 29



CU SIDE AUTHENTICATION WITH EDGE PULSES

FIG. 30

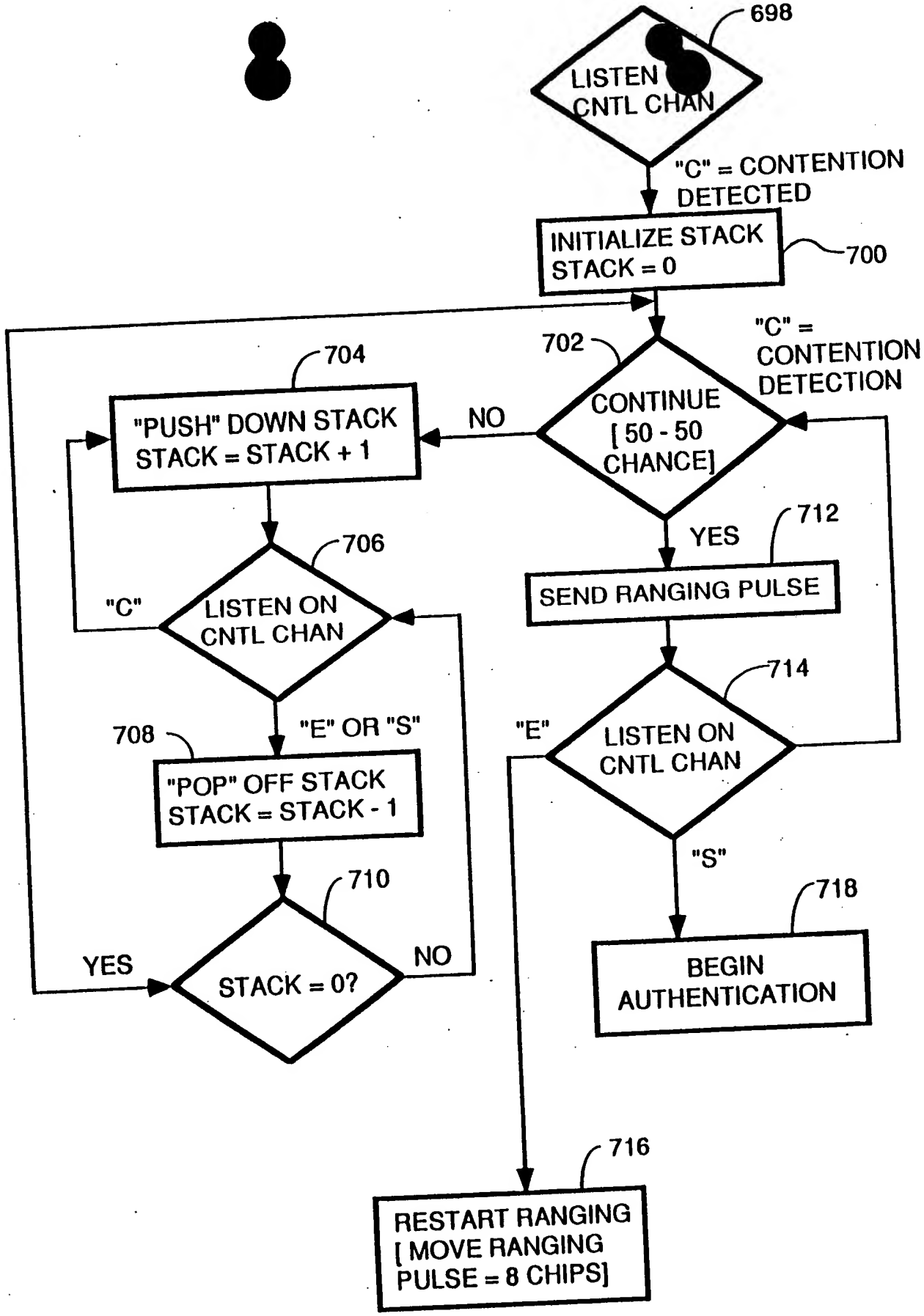


CU RANGING & CONTENTION RESOLUTION

~~RANGING AND CONTENTION RESOLUTION~~
~~CU SIDE~~

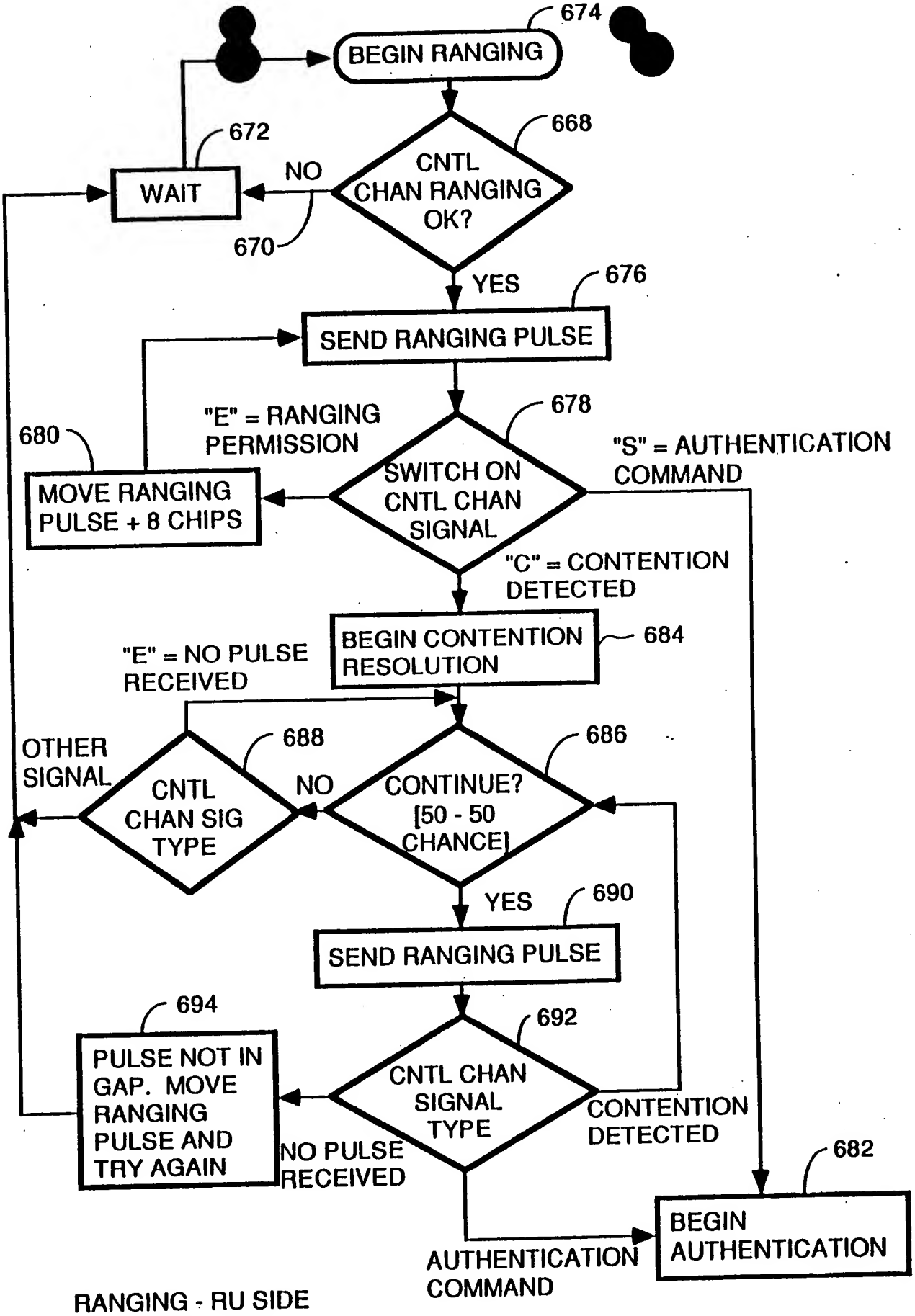
FIG. 31

41



CONTENTION RESOLUTION - RU USING BINARY STACK

FIG. 33



RANGING - RU SIDE
BINARY TREE
ALGORITHM

FIG. 32

50
49

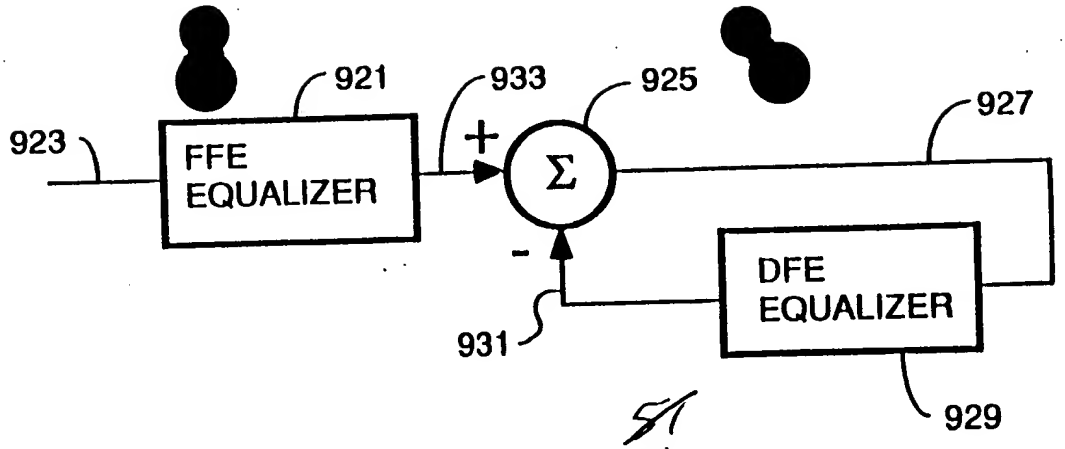


FIG. 37

50

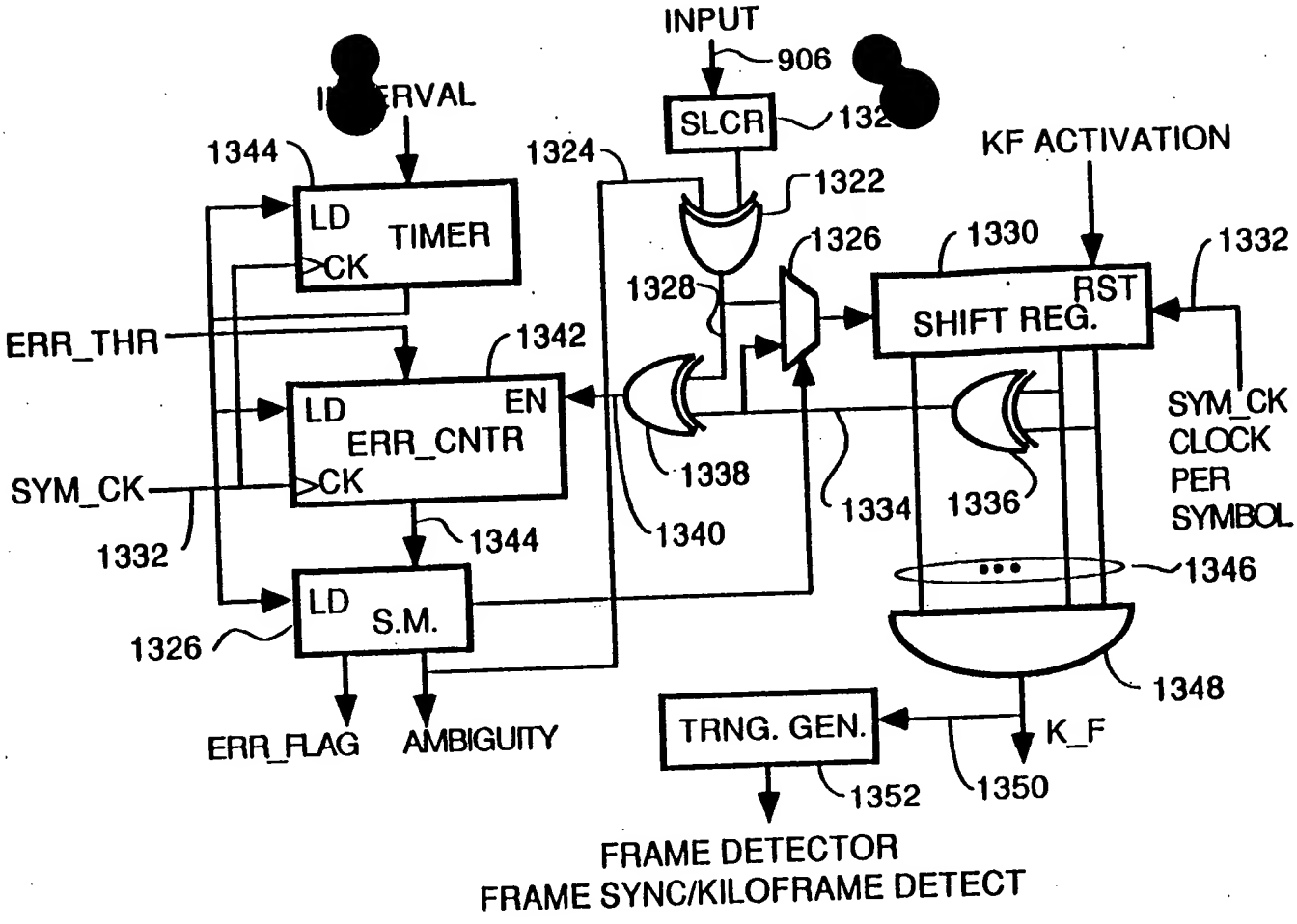
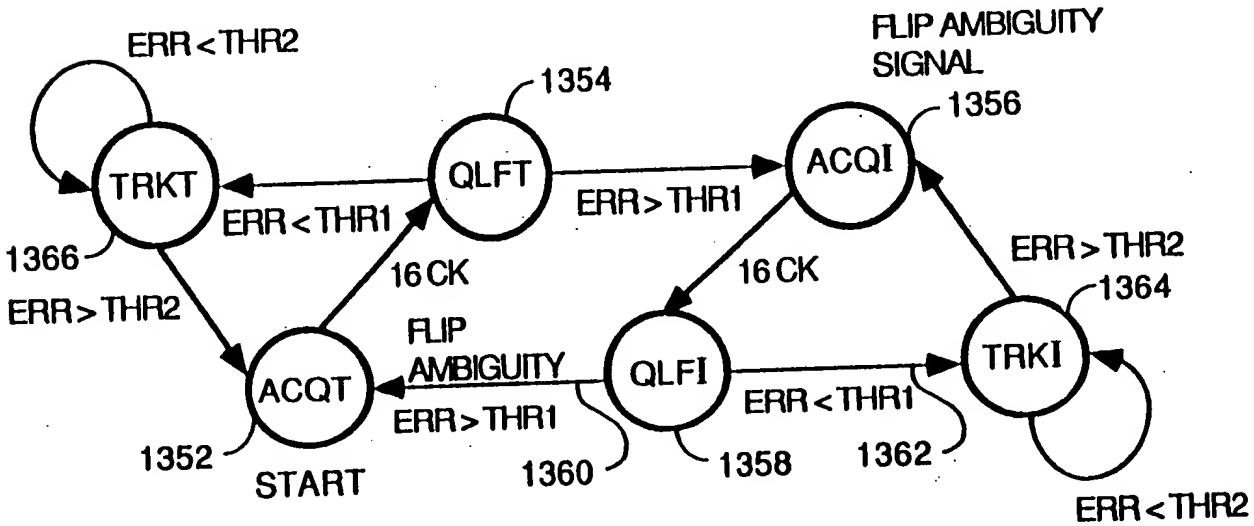


FIG. 52

51



STATE MACHINE

FIG. 53

52

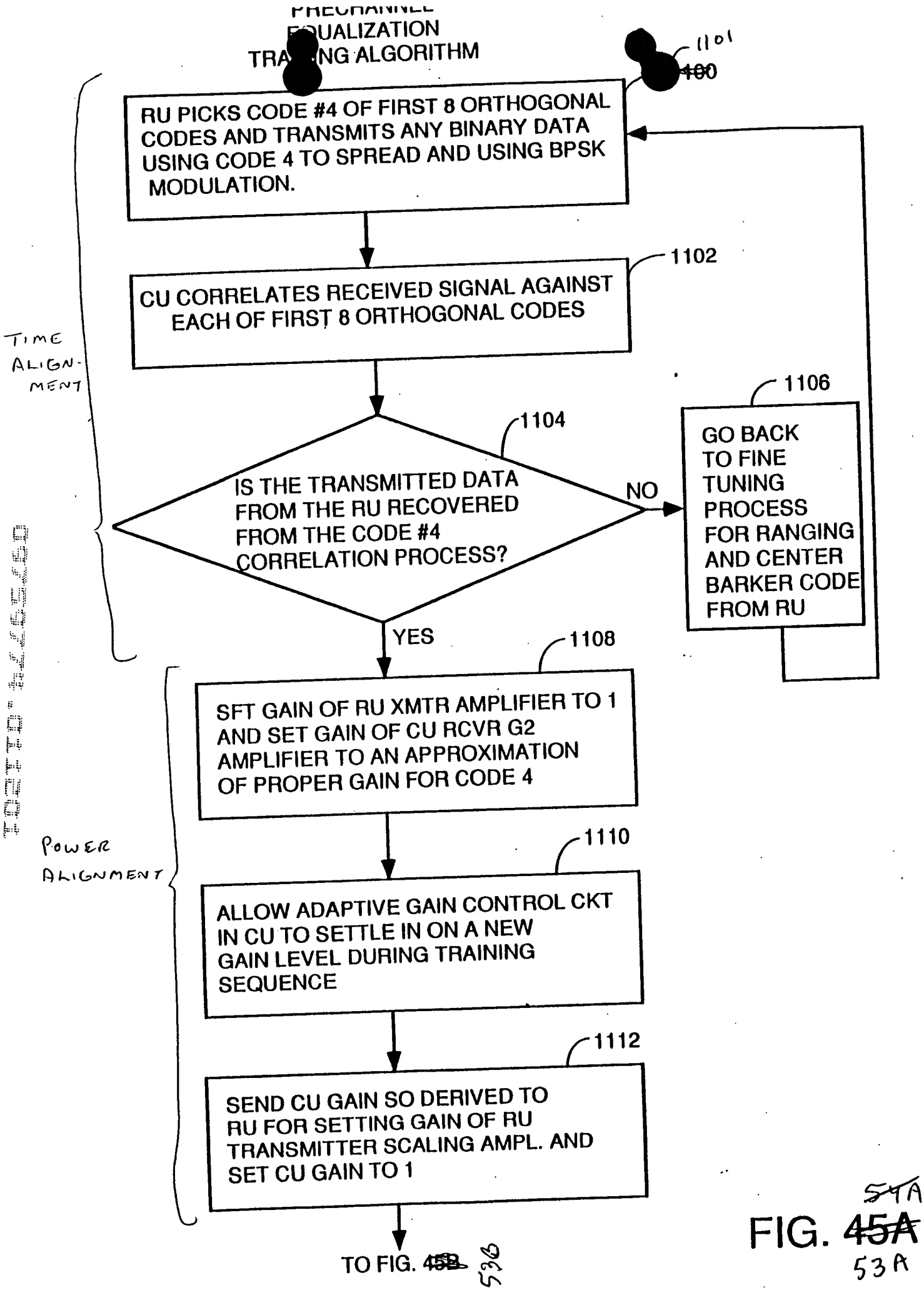

PRECHANNEL
EQUALIZATION
TRAINING ALGORITHM
1101
100
RU PICKS CODE #4 OF FIRST 8 ORTHOGONAL CODES AND TRANSMITS ANY BINARY DATA USING CODE 4 TO SPREAD AND USING BPSK MODULATION.
1102
CU CORRELATES RECEIVED SIGNAL AGAINST EACH OF FIRST 8 ORTHOGONAL CODES
TIME ALIGN-MENT
1104
IS THE TRANSMITTED DATA FROM THE RU RECOVERED FROM THE CODE #4 CORRELATION PROCESS?
NO
1106
GO BACK TO FINE TUNING PROCESS FOR RANGING AND CENTER BARKER CODE FROM RU
YES
1108
SFT GAIN OF RU XMTR AMPLIFIER TO 1 AND SET GAIN OF CU RCVR G2 AMPLIFIER TO AN APPROXIMATION OF PROPER GAIN FOR CODE 4
POWER ALIGNMENT
1110
ALLOW ADAPTIVE GAIN CONTROL CKT IN CU TO SETTLE IN ON A NEW GAIN LEVEL DURING TRAINING SEQUENCE
1112
SEND CU GAIN SO DERIVED TO RU FOR SETTING GAIN OF RU TRANSMITTER SCALING AMPL. AND SET CU GAIN TO 1
TO FIG. 45B
53B

FIG. 45A
53A

FROM FIG. 45A

UPSTREAM EQUALIZATION

1114

CU SENDS MESSAGE TO RU TELLING IT TO SEND EQUALIZATION DATA TO CU USING ALL 8 OF THE FIRST 8 ORTHOGONAL CYCLIC CODES AND BPSK MODULATION.

1116

RU SENDS SAME TRAINING DATA TO CU ON 8 DIFFERENT CHANNELS SPREAD BY EACH OF FIRST 8 ORTHOGONAL CYCLIC CODES.

1118

CU RECEIVER RECEIVES DATA, AND FFE 765, DFE 820 AND LMS 830 PERFORM ONE INTERATION OF TAP WEIGHT(COEFFICIENT) ADJUSTMENTS.

1120

TAP WEIGHT (COEFFICIENT) ADJUSTMENTS CONTINUE UNTIL CONVERGENCE WHEN ERROR SIGNALS DROP OFF TO NEAR ZERO.

1122

AFTER CONVERGENCE DURING TRAINING INTERVAL, CU SENDS FINAL FFE AND DFE COEFFICIENTS TO RU.

1124

RU SETS FINAL FFE & DFE COEFFICIENTS INTO PRECODE FFE/DFE FILTER IN TRANSMITTER.

1126

CU SETS COEFFICIENTS OF FFE 765 AND DFE 820 TO ONE FOR RECEPTION OF UPSTREAM PAYLOAD DATA.

TO FIG. 45C

FIG. ~~45B~~ 54B 53B

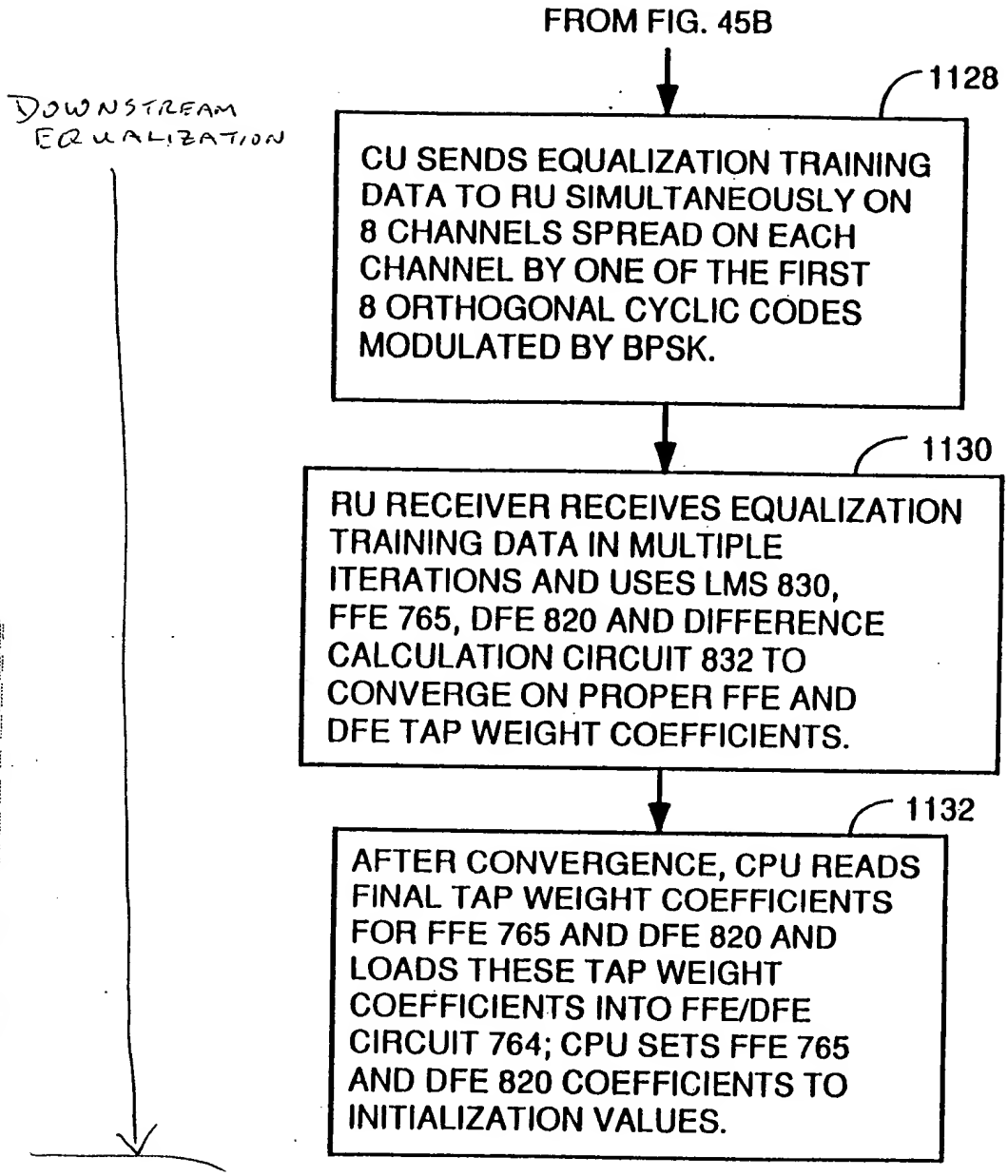


FIG. ~~45C~~ 54C 53C

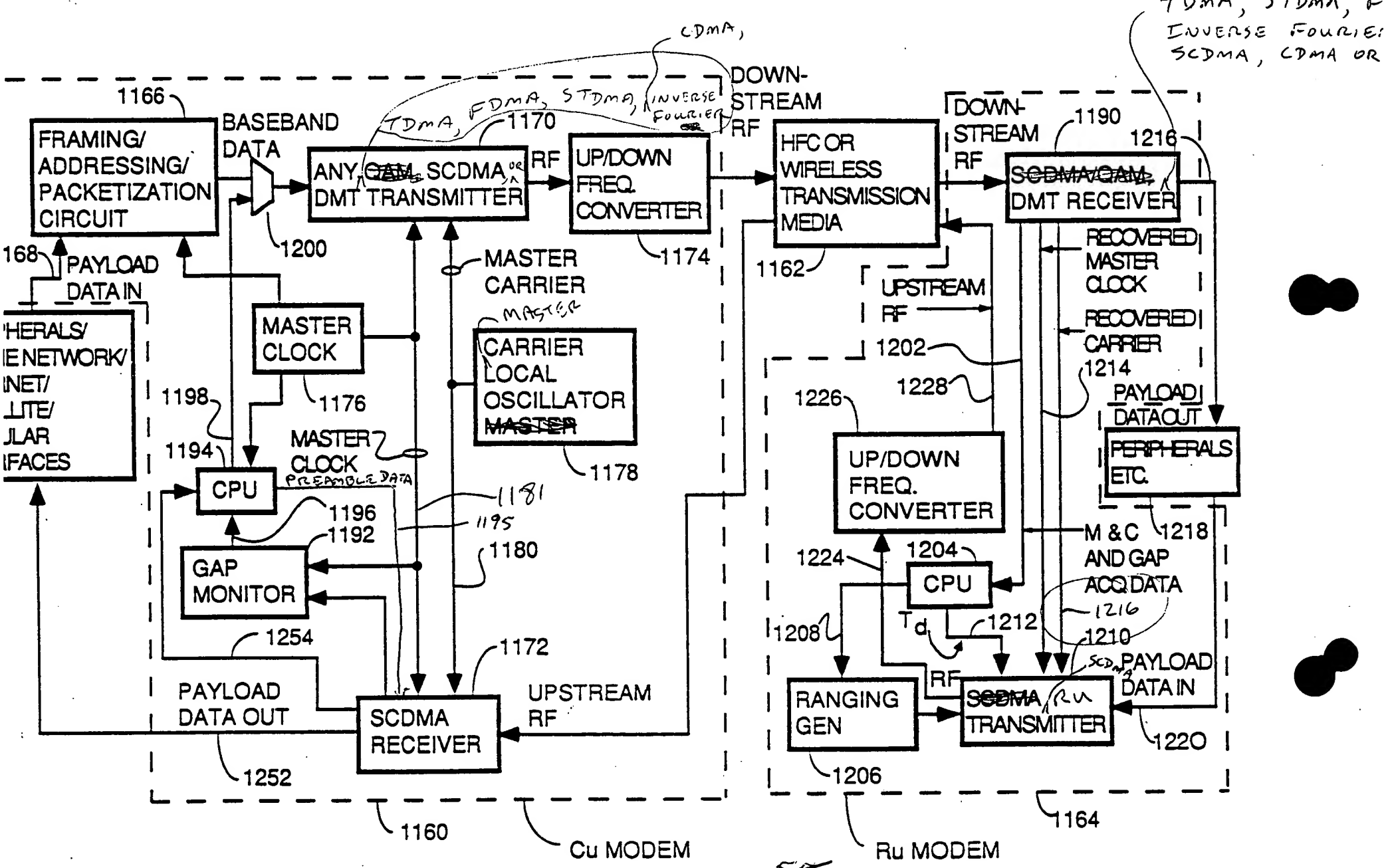
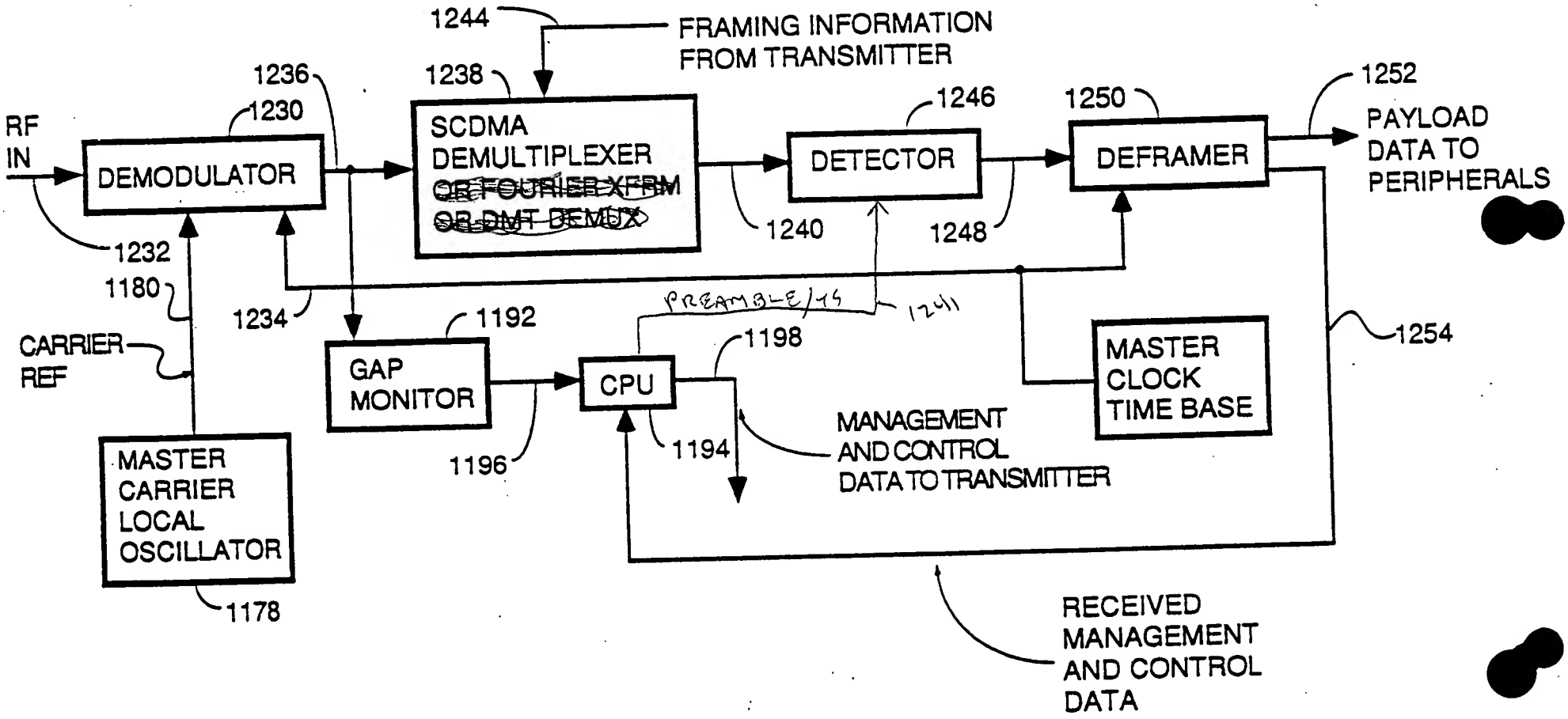

1166
FRAMING/ ADDRESSING/ PACKETIZATION CIRCUIT
BASEBAND DATA
1200
168
PAYLOAD DATA IN
HERALS/ E NETWORK/ INET/ LITE/ JLAR IFACES
MASTER CLOCK
1176
1198
1194
CPU
MASTER CLOCK
PREAMBLE DATA
1196
1192
GAP MONITOR
1254
PAYLOAD DATA OUT
1252
1160
Cu MODEM
1170
ANY, CDMA, SCDMA, OR DMT TRANSMITTER
RF
UP/DOWN FREQ. CONVERTER
1174
MASTER CARRIER
CARRIER LOCAL OSCILLATOR MASTER
1178
1181
1195
1180
1172
SCDMA RECEIVER
UPSTREAM RF
DOWN-STREAM RF
HFC OR WIRELESS TRANSMISSION MEDIA
1162
UPSTREAM RF
1202
1226
UP/DOWN FREQ. CONVERTER
1224
1204
CPU
1208
Td
1212
1210
RANGING GEN
RF
SCDMA RU TRANSMITTER
1220
1206
1164
Ru MODEM
DOWN-STREAM RF
1190
1216
SCDMA/CDMA DMT RECEIVER
RECOVERED MASTER CLOCK
RECOVERED CARRIER
1214
1228
PAYLOAD DATA OUT
PERIPHERALS ETC.
1218
M & C AND GAP ACQ DATA
1216
SCDMA PAYLOAD DATA IN
TDMA, FDMA, STDMA, INVERSE FOURIER OR
CDMA,
TDMA, STDMA, F
INVERSE FOURIE
SCDMA, CDMA OR

FIG. 49

54

TO2TTO'1:2765260

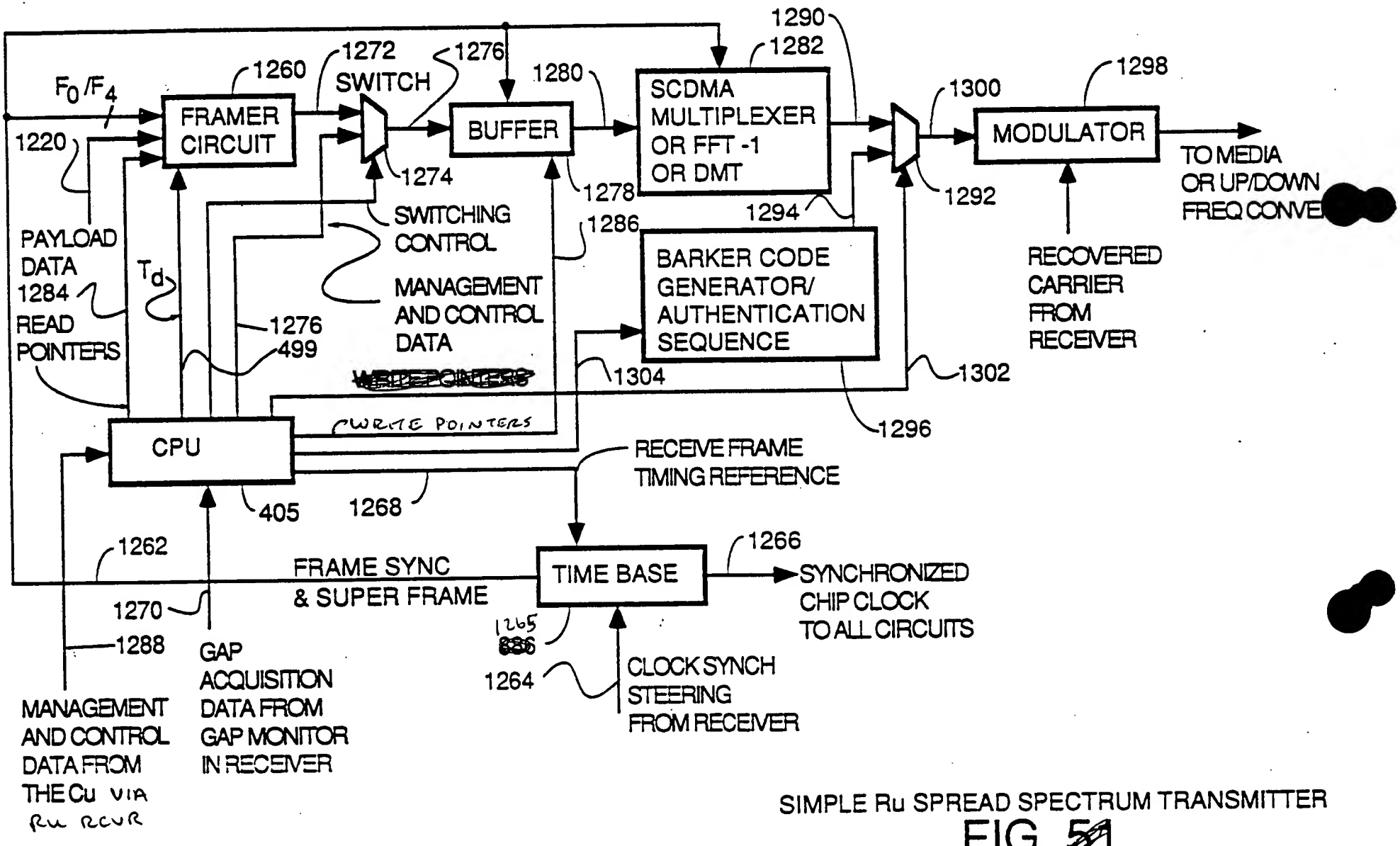


SIMPLE Cu SPREAD SPECTRUM RECEIVER

FIG. ~~50~~ 56

55

TOZITO "4255760

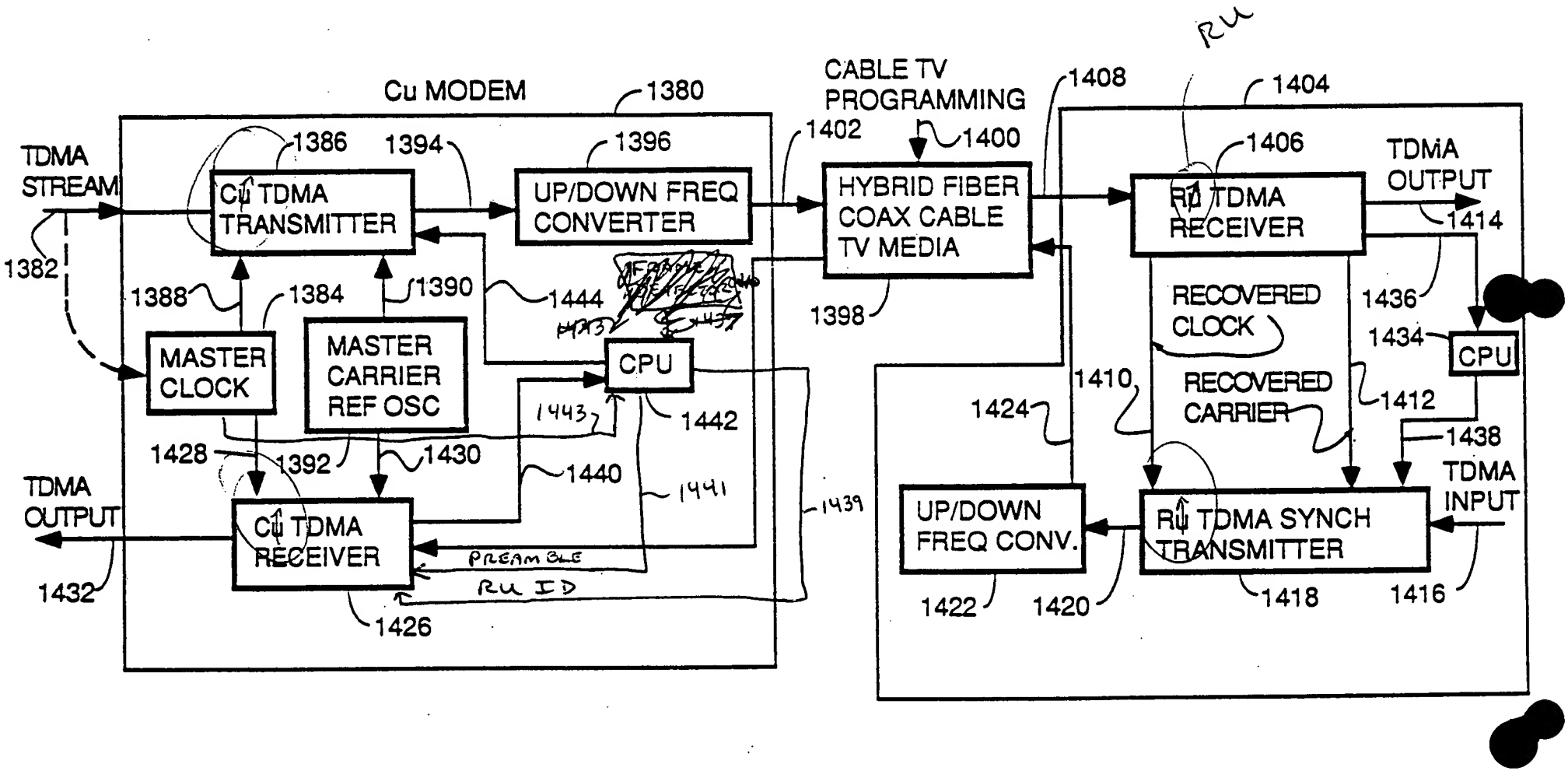


SIMPLE Ru SPREAD SPECTRUM TRANSMITTER

FIG. 51

51

56



SYNCHRONOUS TDMA SYSTEM

FIG. 54

57

OFFSET	1B ASIC		2A ASIC	
(Chips)	RGSRH	RGSRL	RGSRH	RGSRL
0	0x0000	0x8000	0x0001	0x0000
1/2	0x0000	0xC000	0x0001	0x8000
1	0x0000	0x4000	0x0000	0x8000
-1	0x0001	0x0000	0x0002	0x0000

FIG. 58

Training Algorithm

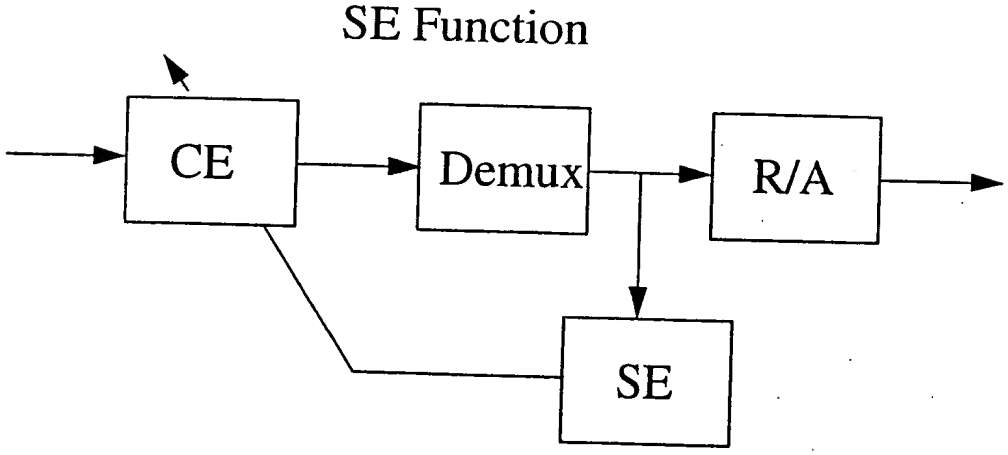
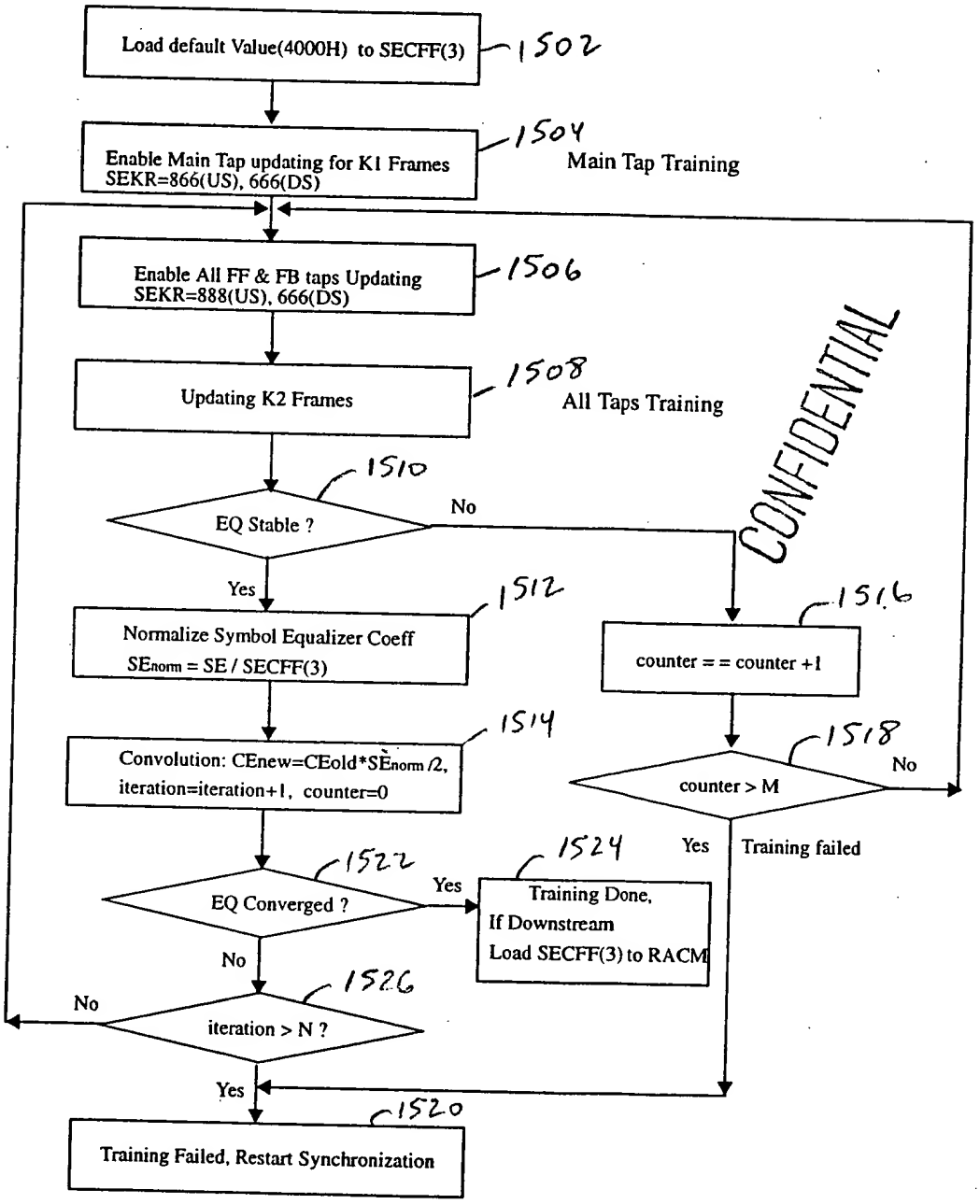


FIG. 59

Initial 2-Step Training Algorithm



2-STEP INITIAL EQUALIZATION TRAINING

FIG. 60

CONFIDENTIAL

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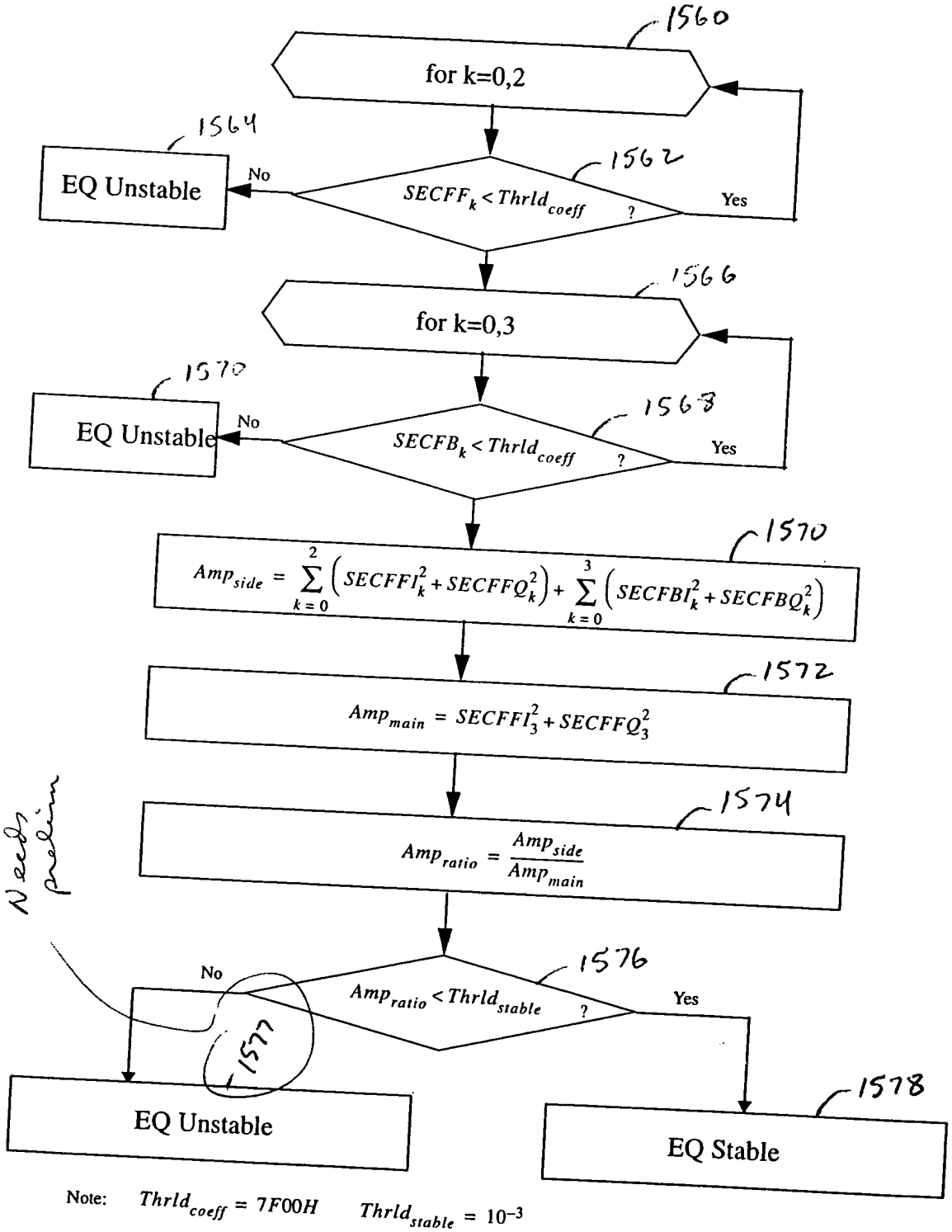
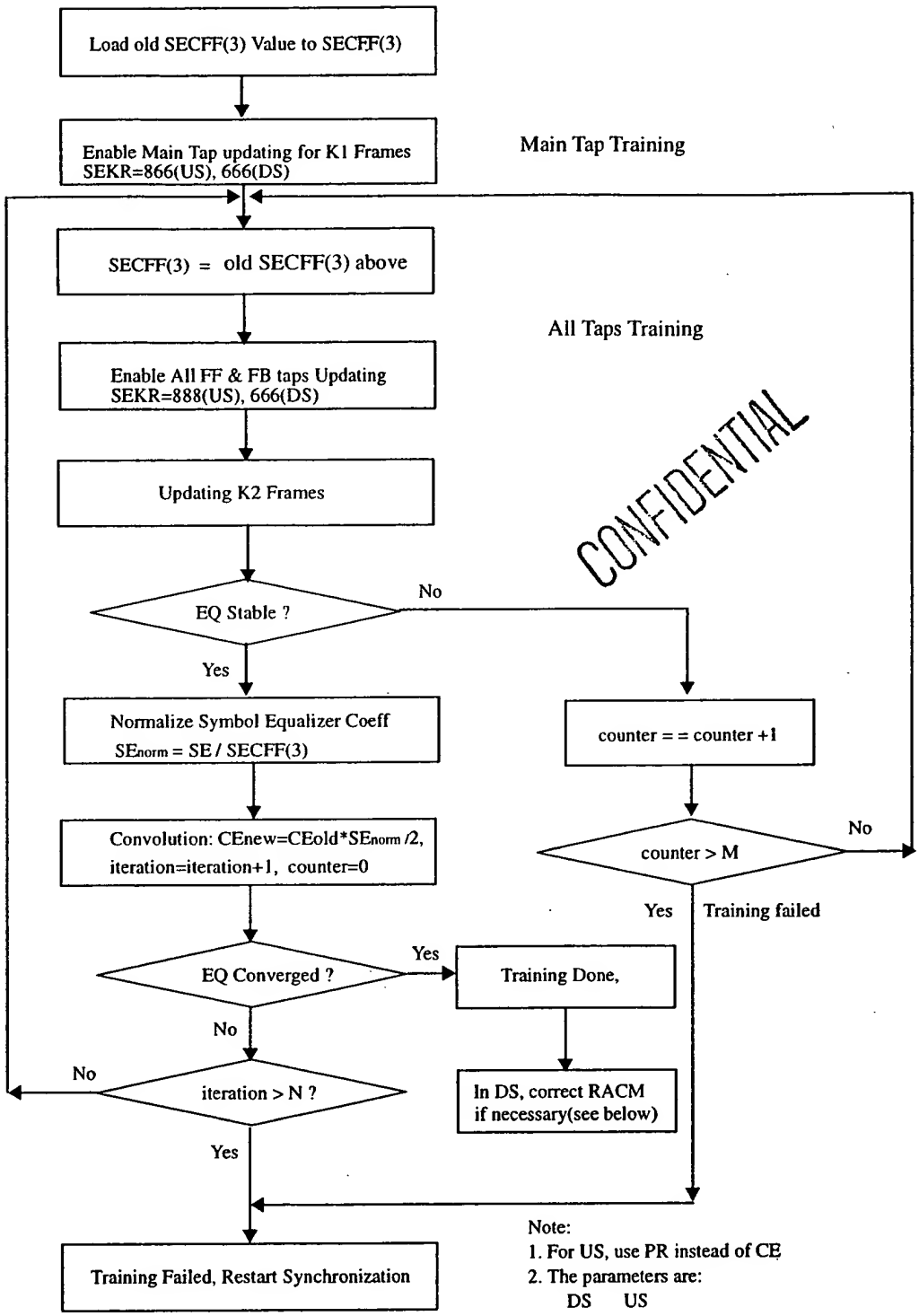
EQ Stability Check



Note: $Thrld_{coeff} = 7F00H$ $Thrld_{stable} = 10^{-3}$

FIG. 61

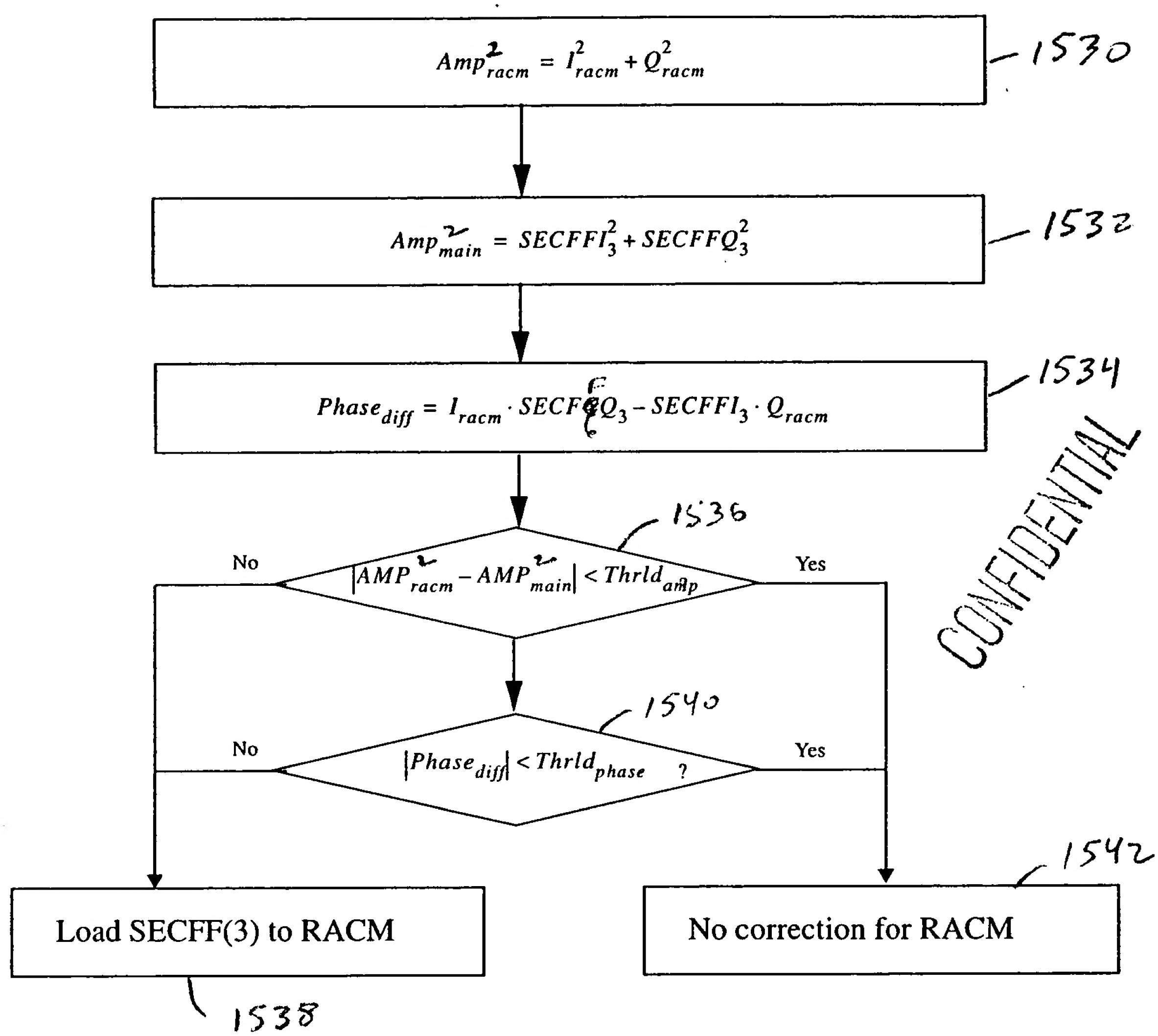
Periodic 2-Step Training Algorithm



CONFIDENTIAL

FIG. 62

RACM Correction



Note: $Thrld_{amp} = TBD$

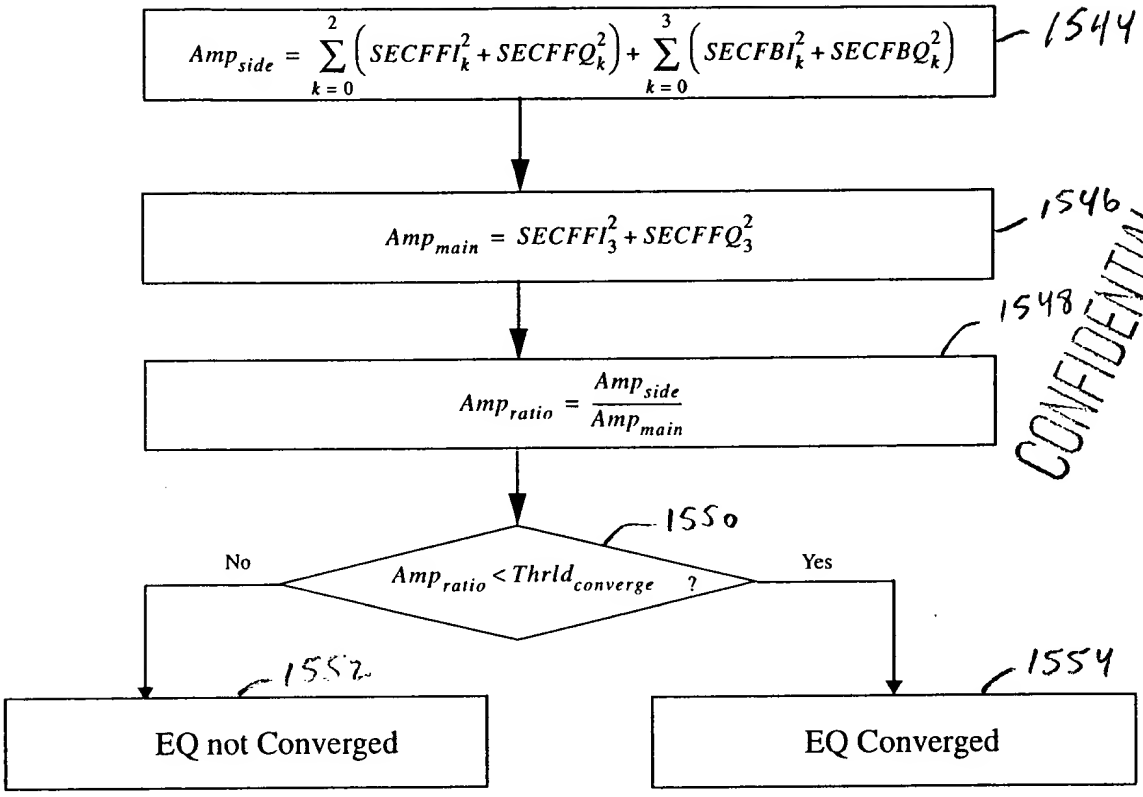
$Thrld_{phase} = TBD$

CONFIDENTIAL

ROTATIONAL AMPLIFIER CORRECTION

FIG. 63

EQ Convergence Check



Note: $Thrld_{converge} = 10^{-5}$

FIG. 64

CONFIDENTIAL

Power Alignment Flow Chart

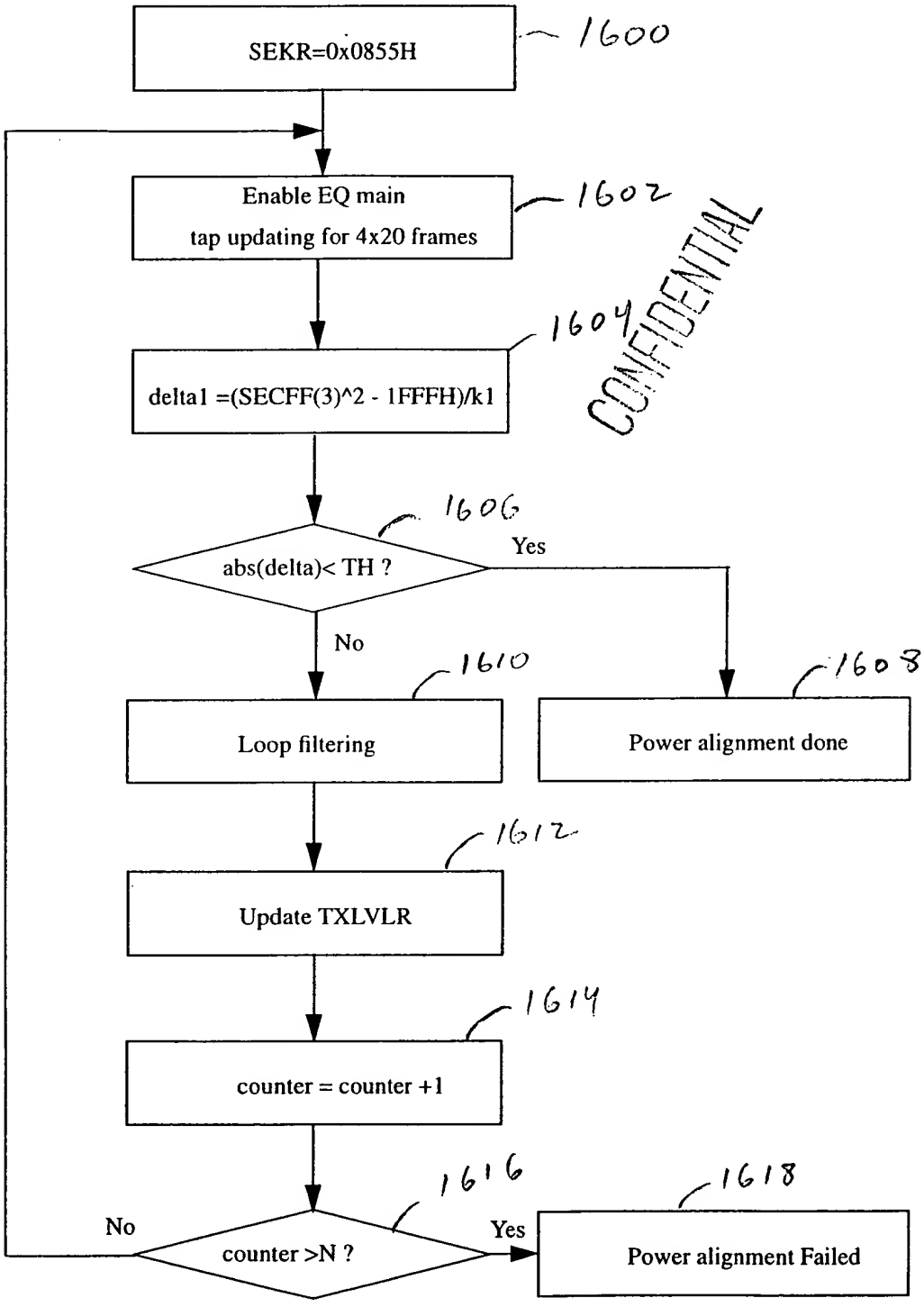


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FIG. 65

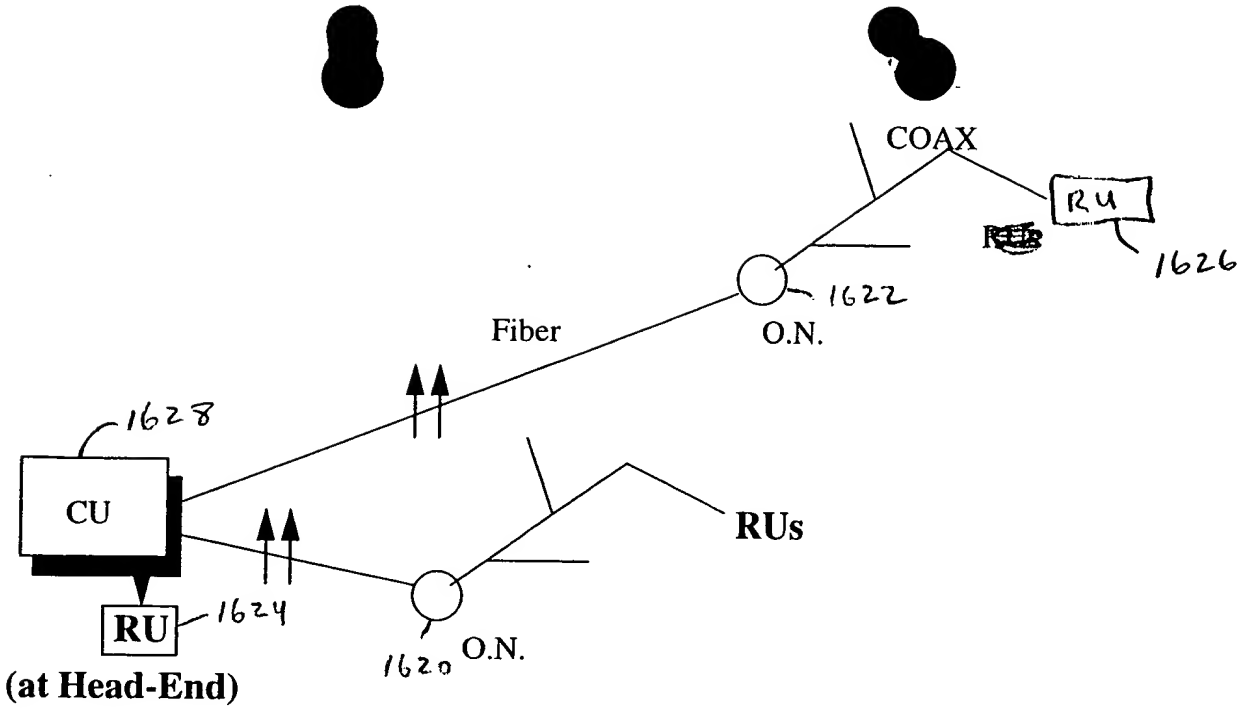
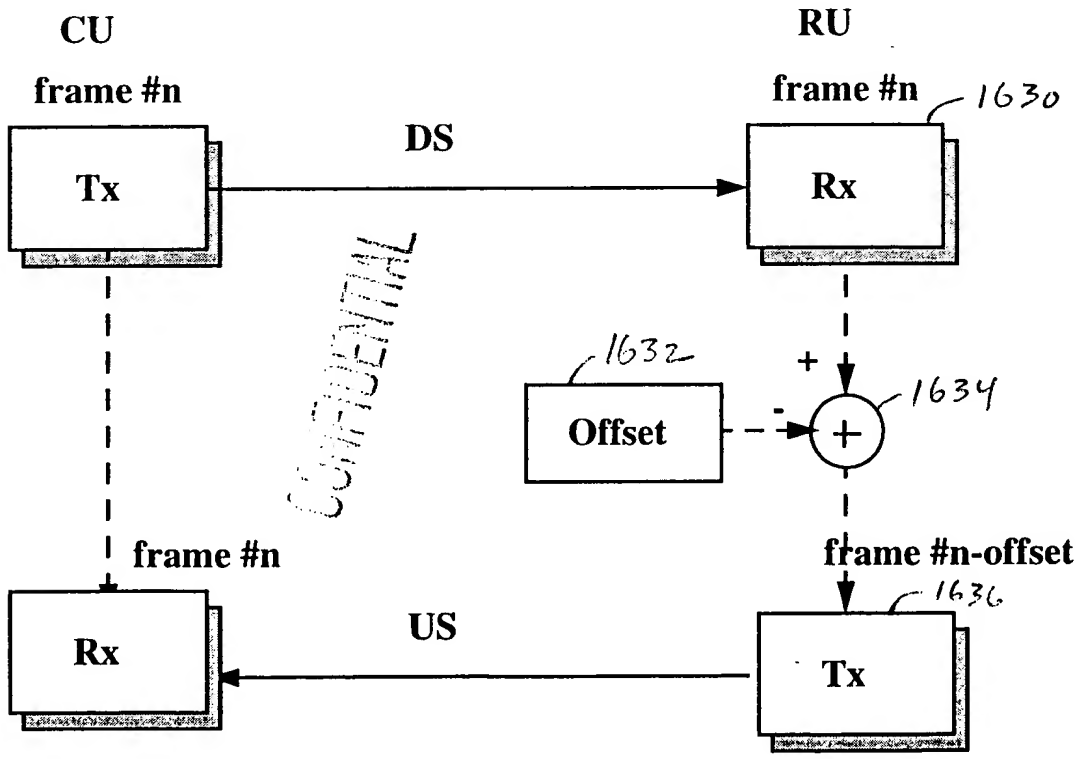


FIG. 66



Total Turn Around (TTA) in frames = Offset

FIG. 67

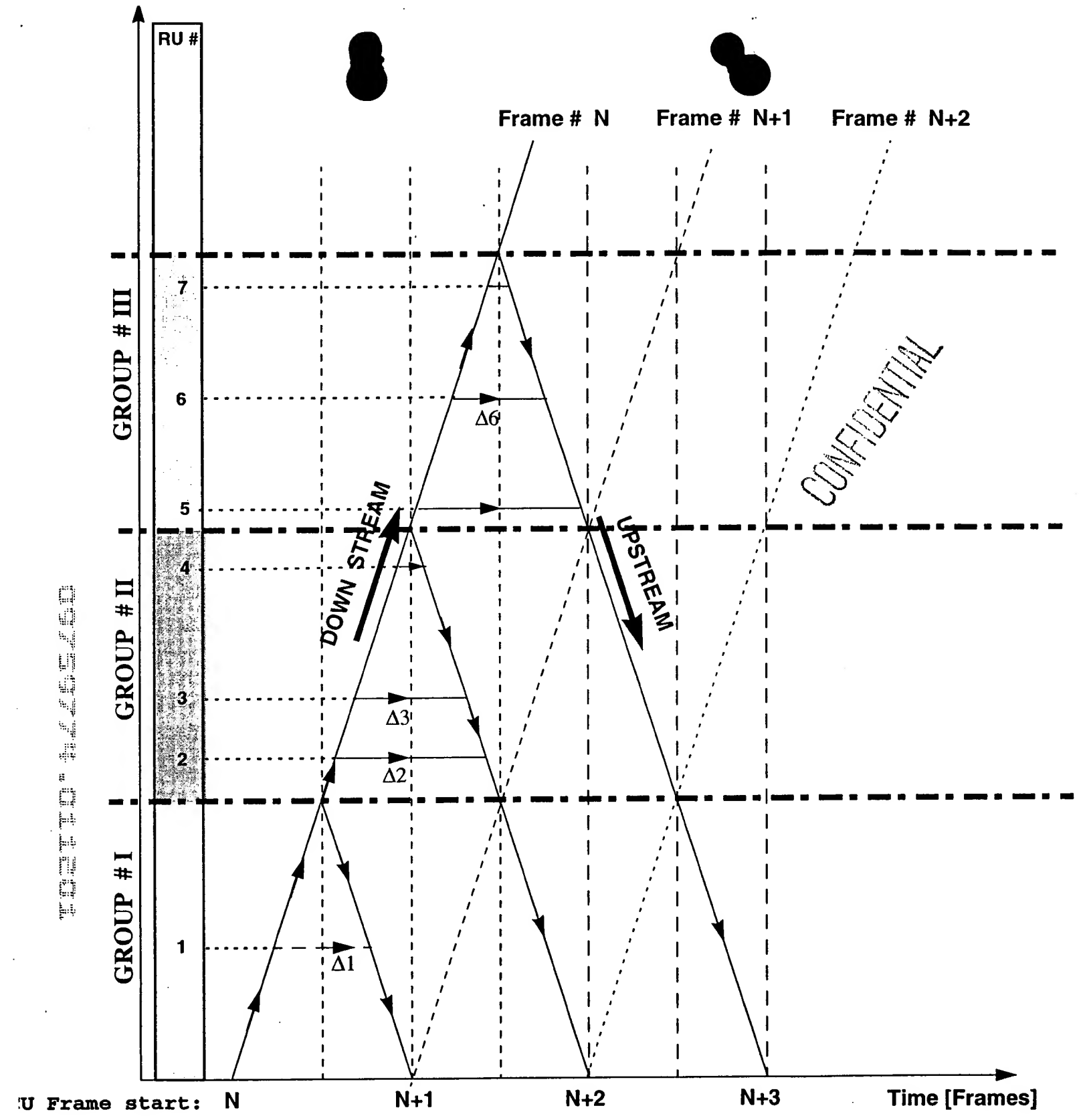


FIG. 6B

Figure 3.1: Frame start propagation along the channel

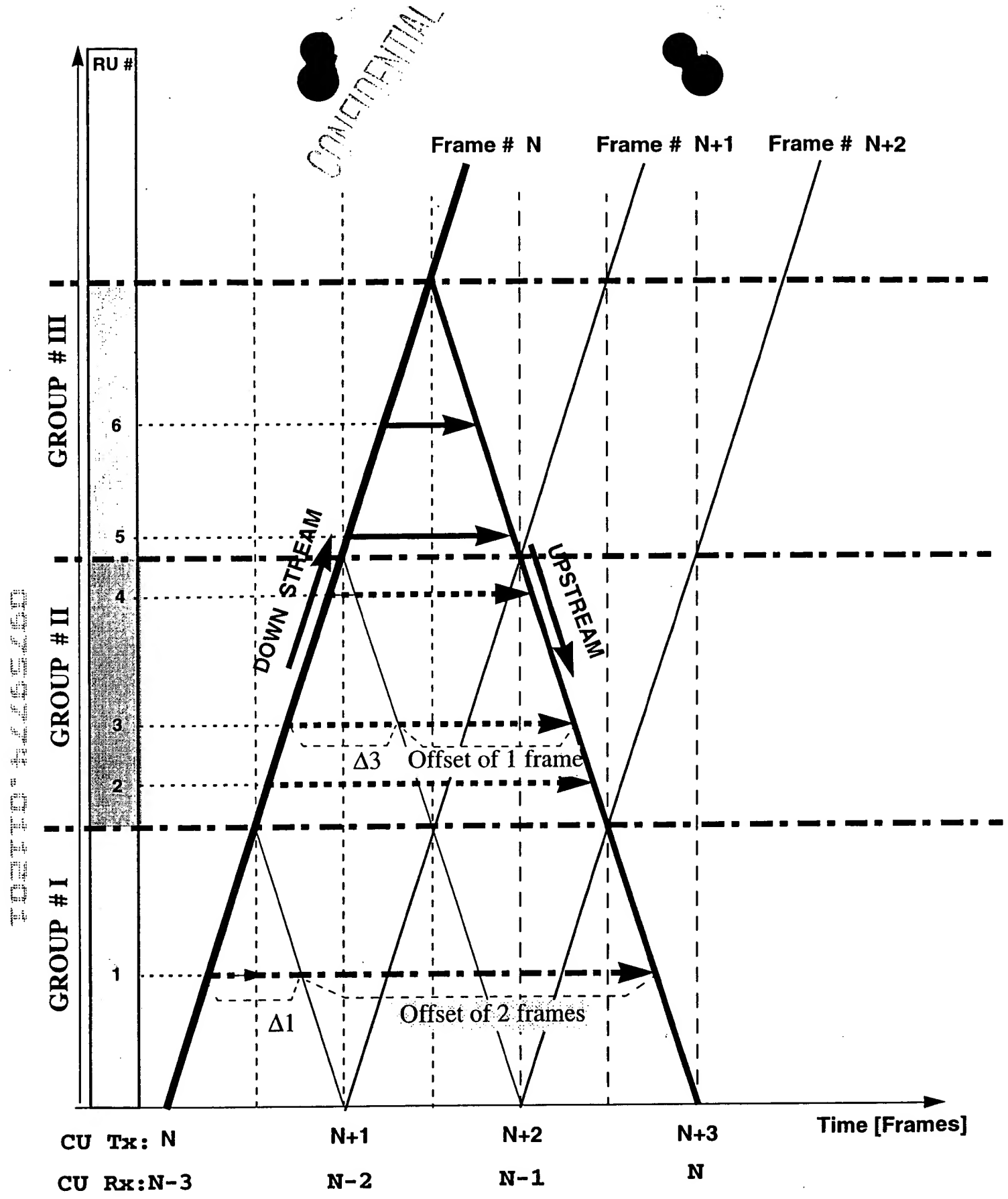


FIG. 69

Figure 69 Control message (downstream) and function (upstream) propagation in a 3 frames TTA channel

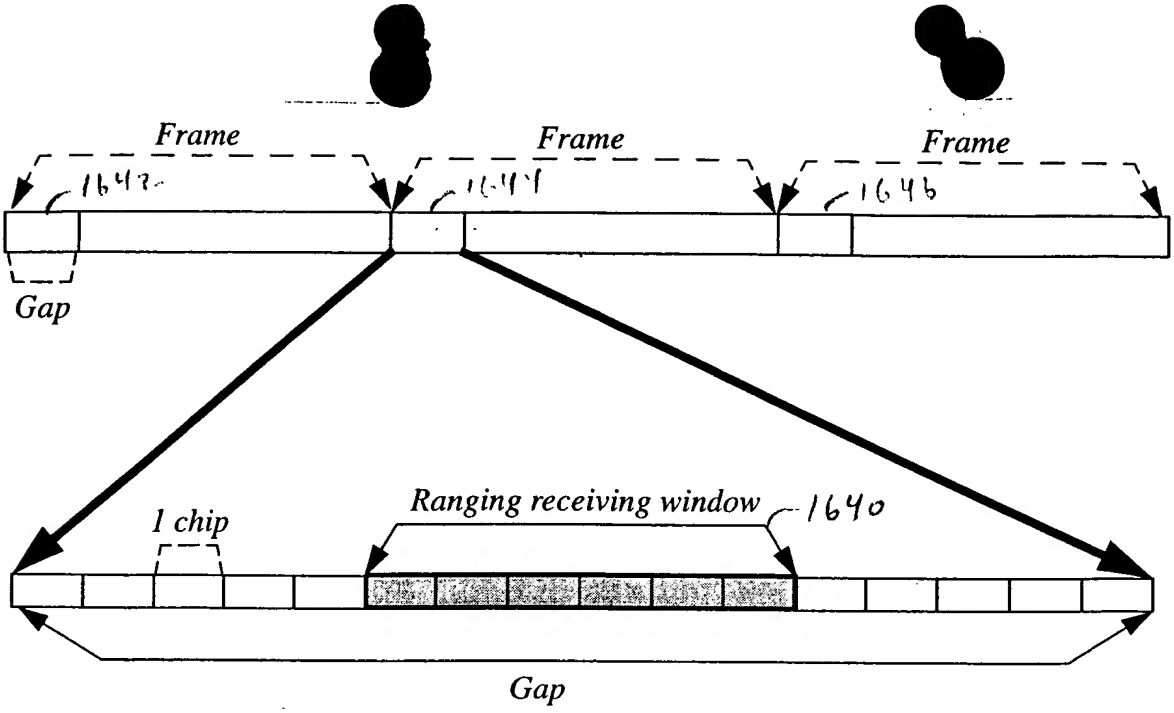


FIG. 70

PATENT APPLICATION

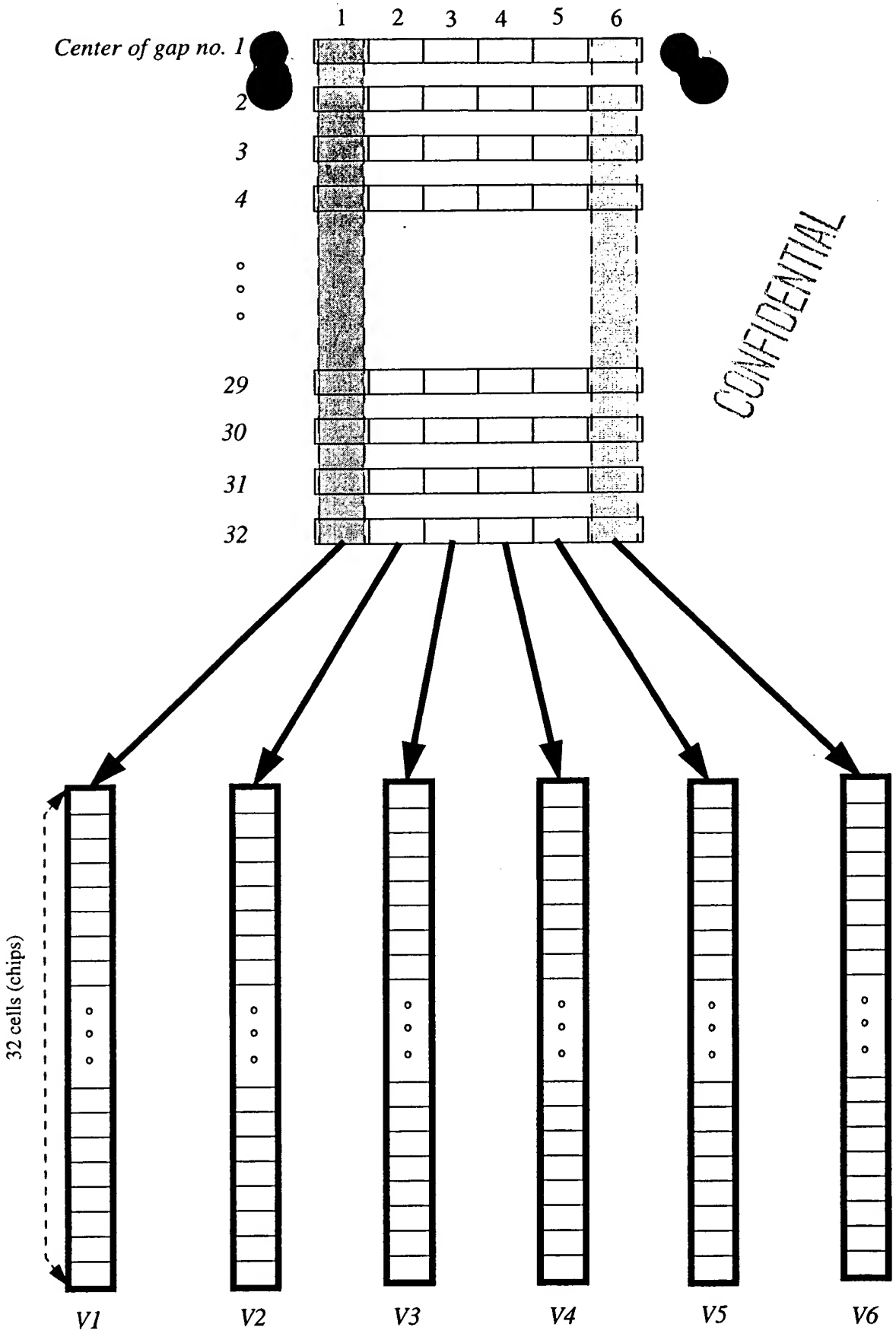


Figure 3.4: Overall view of the CU sensing windows in a "boundless ranging" algorithm

FIG. 7I

6

Chip\FR	1	2	3	4	5	6	7		33
1	**0**	**0**	**1**	**0**	**0**	**1**	**1**	**...**	**0**
2	1	0	0	1	1	1	1	...	
3	0	0	0	1	1	1			
4	0	0	0	1	0	0	0	...	0
5	0	1	0	0	1				
6	0	0	1	1	1				
7	0	0	0	1	1				
8	0	0	0	0	1	0	0	...	

FIG. 72